Sequential Circuits-II

Lesson: Sequential Circuits-II

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4.1 Chapters Objective

- Introduction to edge triggered flip-flops
- To design edge triggered S-R, D, J-K Flip-flop.
- To explain how edge triggered and master slave flip-flop differ.
- To study about asynchronous inputs
- To understand the flip-flop operating characteristics such propagation delays, set-up time and hold time.
- To study the basic applications of flip-flop.

4.2 Introduction

4.2.1 Edge-triggered flip-flops

In digital applications two mode of operations are popular, one is asynchronous mode of operation and other is synchronous mode of operation. In the former, the output of the logic circuit can change its state at anytime whenever the input changes. The details of such a mode will be discussed in later sections. In synchronous mode of operation, the exact time at which the output can change its state can be predetermined by clock signal. The clock signal is distributed to all part of the system and most of the system outputs can change state only when the clock makes a transition. The transitions are also called as edges. When there is a transition from 0 to 1 it is named as positive edge triggered and when the clock pulse makes a transition from high to low i.e. from 1 to 0 it is termed as negative edge triggered. In the figure 1 the blue colored transitions are the positive edge and red colored transitions are the negative edge.

Figure 1: Edge transitions in a clock pulse

Thus edge triggering is sensitive only at the transitions of the clock. Positive edge triggering is indicated by a triangle at the clock terminal of the flip-flop. Negative edge triggering is indicated by a triangle with a bubble at the clock terminal of the flip-flop. Different types of edge triggered flip-flop include edge-triggered S-R flip-flop, D flip-flop and J-K flip-flop.

Edge-triggered S-R flip-flop

The logic symbol of positive edge triggered S-R flip flop is given in figure 2.

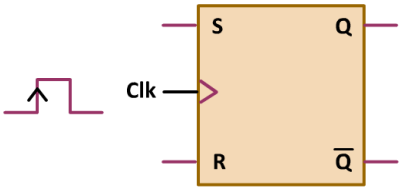

Figure 2: Logic symbol of positive edge triggered S-R Flip-flop

Table 1 gives the truth table for positive edge triggered S-R flip-flop. The S and R inputs of the flip-flop are synchronous control input as the output changes with respect to the input only on the positive edge of the clock pulse. When there is no clock pulse or even at the trailing edge (shown in red dotted line of figure 1) then S and R inputs have no effect on the output. However at the positive edge/leading edge of the clock the flip-flop become active and follows the change in S and R input. When S is high and R is low then the output goes HIGH at the positive edge of the clock pulse and SET the flip-flop. When S is low and R is high then the output goes LOW at the positive edge of the clock pulse and RESET the flip-flop. When both the inputs are low the output retains its previous state and observes no change, at the leading edge of the clock pulse. When both inputs are high the flip-flop is in forbidden state.

CLK	S	R	Q_{n+1}	Remarks
0	X	X	Q_n	No change
↑	0	0	Q_n	No change
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	?	Forbidden state

Table 1: Truth table for positive edge triggered S-R flip-flop

The logic symbol and the truth table of negative edge triggered S-R flip flop is given in figure 3.

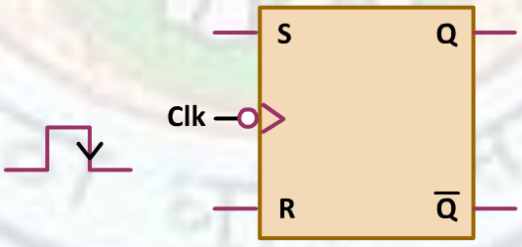

Figure 3: Logic symbol of negative edge triggered S-R Flip-flop.

The S and R inputs of the flip-flop are synchronous control input as the output changes with respect to the input only on the negative edge of the clock pulse. The output of the flip-flop will follow the changes at the input, only when the clock pulse makes a transition from 1 to 0. Table 2 gives the truth table for negative edge triggered S-R Flip-flop.

CLK	S	R	Q_{n+1}	Remarks
↓	0	0	Q_n	No change
↓	0	1	0	Reset
↓	1	0	1	Set
↓	1	1	?	Forbidden state

Table 2: Truth table for negative edge triggered S-R Flip-flop.

Try yourself

The waveform shown in the figure is applied to the positive edge triggered S-R flip-flop which is assumed to be initially RESET. Sketch the output waveform.

Solution

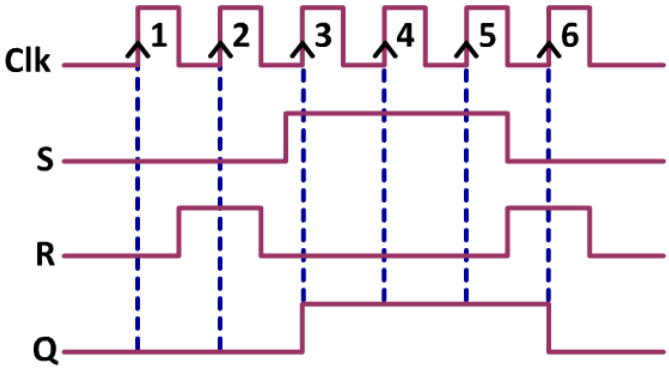

Figure 4: Timing diagram

The output waveform is given in the figure 4 and is explained as follows

1. During the first positive clock edge, S=R=0 so the output will retain its last state. As the flip-flop is assumed to be RESET so the output will remain zero till next positive edge arrives.
2. During second positive clock edge, S=0 and R=1, the output still remains zero till next positive clock edge arrives.
3. During third positive clock edge, S=1 and R=0, the output will become high and will remain at high till next positive clock edge arrives.
4. During fourth positive clock edge, S=1 and R=0, the output remains at high and will remain at high till sixth positive clock edge arrives as same input condition prevails even at fifth clock pulse.
5. During sixth positive clock edge, S=0 and R=1, which will force the output to be low and it will remain at low till next positive clock edge arrives.

Edge-triggered D flip-flop

By now students got the idea that edge triggered flip-flop are triggered only at the positive/leading edge or negative/trailing edge of the clock pulse. The beauty of such a circuit lies in the fact that flip-flop samples the data only at a unique point in time unlike in clocked flip-flop where the output can change at any time when the clock is still high. In order to avoid such a condition it is necessary that the clock pulse should be modified. Instead of being a rectangular pulse if the clock can be designed in form of spikes then the probable of false triggering can be avoided. Figure 5 shows the new clock trigger which can be designed using a simple RC differentiator circuit.

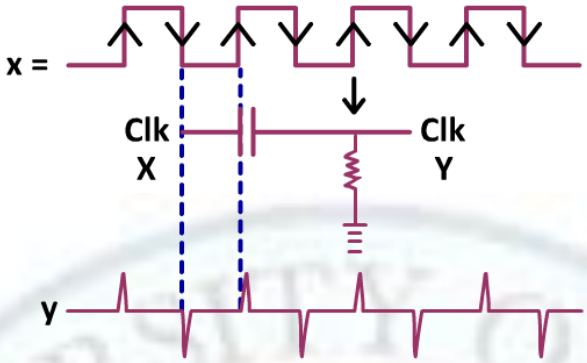

Figure 5: Generating spikes from clock pulse

Figure 5 shows the RC differentiator circuit which is normally designed to generate clock input for D flip-flop. In the RC differentiator circuit, RC time constant is made much smaller that the clock pulse width. Because of very small time constant the capacitor charges immediately when the clock goes high. This exponential charging of capacitor produces a narrow positive spike across the resistor. Similarly capacitor discharges fully at the trailing edge of the clock pulse resulting in narrow negative spike.

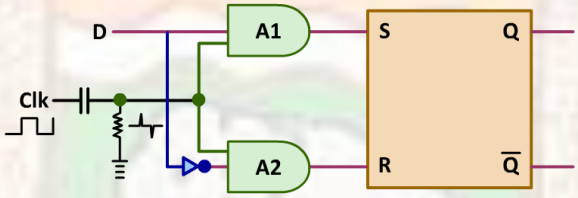

Figure 6: Edge triggered D Flip-flop

The narrow positive spike activates the AND gates A1 and A2 for an instant and samples the value of D input at that instant. It can be seen from the figure 6 that exactly when positive spike hit the AND gates, D and its compliment hit the flip-flop. The flip-flop will SET and RESET as the value of D is at logic 1 or logic 0 respectively. When the negative spike hit the flip-flop then both the AND gates are disabled and the output of both A1 and A2 are at logic 0. Since both S and R input are at logic 0 so output will retain the last state and observes no change. It can be observed from the truth table that during negative spike of clock signal the D input has no significance and the output becomes independent of the value of D input. This mode of operation is termed as edge triggering because the flip-flop responds only when the clock is in transition between the two voltage states. Table 3 gives the truth table for the positive edge triggered D Flip-flop.

CLK	D	Q_{n+1}	Remarks
0	X	Q_n	No change
↑	0	0	Reset

↑	1	1	Set
↓	X	Q_n	No change

Table 3: Truth table for the positive edge triggered D Flip-flop.

The negative edge triggered D flip-flop operates in the same way as a positive edge triggered D flip-flop except that the change of state takes place at the negative going edge of the clock pulse. Figure 7 shows the logic symbol of negative edge triggered flip-flop. Table 4 gives the truth table for the negative edge triggered D Flip-flop.

CLK	**D**	**Q_{n+1}**	**Remarks**
↓	0	0	Reset
↓	1	1	Set
↑	X	Q_n	No change

Table 4: Truth table for the negative edge triggered D Flip-flop.

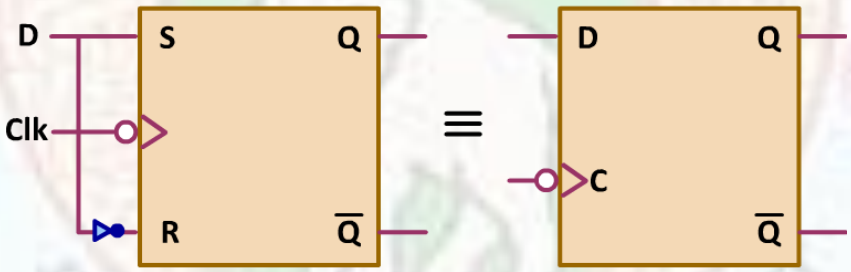

Figure 7: Logic symbol of negative edge triggered D Flip-flop.

Try yourself

The waveform shown in the figure 8 is applied to the negative edge triggered D flip-flop which is assumed to be initially SET. Sketch the output waveform.

Solution

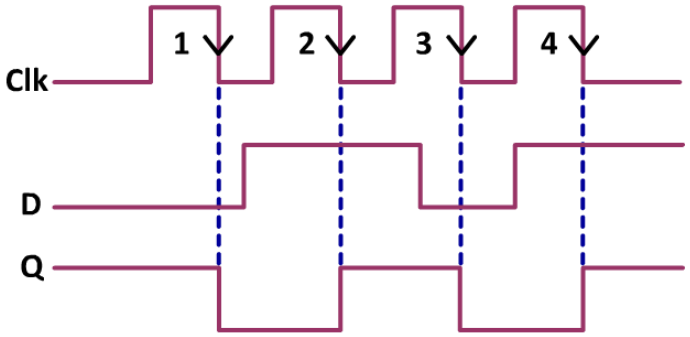

Figure 8: Timing diagram

The output waveform is given in the figure 8 and is explained as follows

1. During the first negative clock edge, D=0 so the output which is initially SET will now change to logic 0.
2. During the second negative clock edge, D=1 so the output goes high.
3. During the third negative clock edge, D=0 so the output goes low.
4. During the fourth negative clock edge, D=1 so the output goes high.

Edge-triggered J-K flip-flop

The functioning of edge triggered J-K flip-flop is similar to edge triggered S-R Flip-flop except the last state when both the inputs are high. In case of edge triggered J-K flip-flop the output toggles i.e. goes to the opposite state at the positive going edge of the clock, when both the inputs are high unlike in S-R flip-flop where it is a forbidden state. Figure 9 shows the circuit diagram and the logic symbol of positive edge triggered J-K flip-flop.

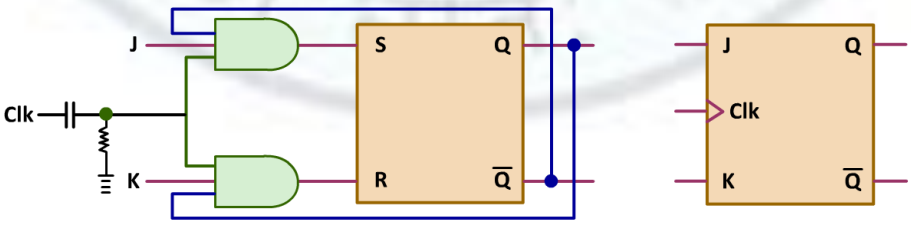

Figure 9: Circuit diagram and logic symbol of positive edge triggered J-K flip-flop.

Table 5 shows the truth table of positive edge triggered J-K flip-flop.

CLK	J	K	Q_{n+1}	Remarks
0	X	X	Q_n	No change
↑	0	0	Q_n	No change
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	$\overline{Q_n}$	Toggle

Table 5: Truth table for positive edge triggered J-K flip-flop.

Try yourself

The waveform shown in the figure 10 is applied to the negative edge triggered J-K flip-flop which is assumed to be initially RESET. Sketch the output waveform.

Solution

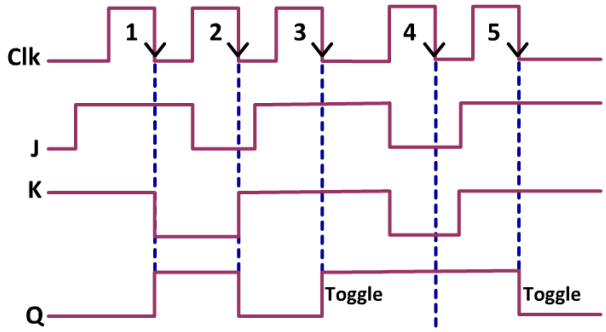

Figure 10: Timing diagram

The output waveform is given in figure 10 and is explained as follows

1. During the first negative clock edge, J=1 and K=0 so the output which is initially RESET will now change to logic 1.
2. During the second negative clock edge, J=0 and K=1 so the output goes low.
3. During the third negative clock edge, J=K=1 so the output toggles i.e. initially it was in low state now the output goes high.
4. During the fourth negative clock edge, J=K=0 so the output retains its last value which is a high state.
5. During the fifth negative clock edge, J=K=1, the output will toggle, the last state was high so at fifth negative clock edge the output goes low.

What would the Q output look like if the J and K waveforms are inverted

Race around condition

A common problem associated with J-K flip-flop is racing. Racing or race around condition means toggling more than once during a clock pulse. For example when the inputs J=K=1 and assuming that Q=0 then a clock pulse as shown in the figure 11 is applied at the clock input of J-K flip-flop.

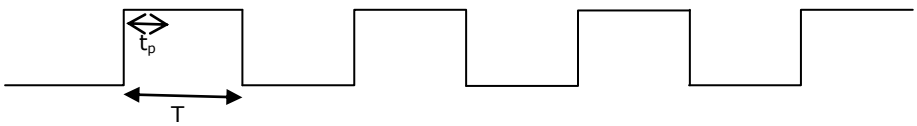

Figure 11: Clock input of J-K flip-flop with t_p<T

After the propagation delay time (t_p) (see section 4.6) taken by the gates in J-K flip-flop the output will toggle and the new output will be Q=1, if the previous output was 0. The inputs remains same i.e. J=K=1 with Q=1 as the output. So after another time interval of t_p sec the output will again toggle as the clock input is still high, changing back to Q=0. Thus the output oscillates back n forth between 0 and 1 after every t_p second. This situation is referred to as the race around condition.

How to avoid racing

- Propagation delay can prevent J-K flip-flop from racing. If somehow t_p>T then racing condition can be avoided. From the figure 12 it can be understood that

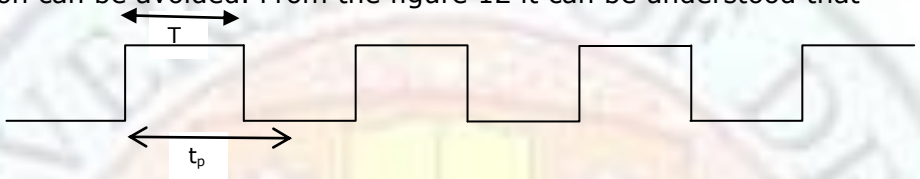

Figure 12: Clock input of J-K flip-flop with t_p>T

If t_p>T, the output change approximately t_p sec after the leading edge of the clock. As the clock width is narrower than t_p sec, the returning Q and $\bar{Q}$ arrive too late to cause false triggering thus avoiding toggling more than once during a clock pulse and thereby avoids racing condition. Generally it is difficult to satisfy the condition t_p>T because of very small propagation delays in IC.

- Another practical way of avoid racing is to use edge triggering or to use master-slave flip-flop.

J-K Master-Slave flip-flop

J-K Master-Slave flip-flop is a pulse triggered flip-flop. Data are entered into the flip-flop at the leading edge of the clock pulse but the output does not reflect the input state until the trailing edge. The master is active when the clock is high and the slave is inactive during that time. Slave becomes active and master becomes inactive when the clock is low. The pulse triggered Master-Slave flip-flop does not allow data to change while the clock pulse is active. The logic symbol of J-K Master-Slave flip-flop is shown in the figure 13. The symbol ⌝ signifies that the output does not reflect the input data until the occurrence of the clock edge (either leading edge or trailing edge) following the triggering edge.

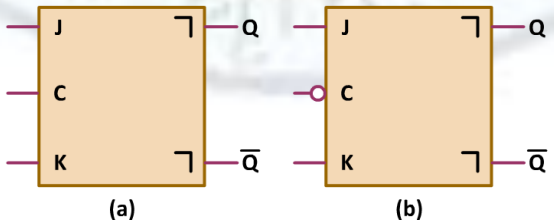

Figure 13: Logic symbol of Pulse triggered J-K Master slave flip-flop a) Active high clock: Data are clocked in on positive-going edge of clock pulse and transferred to output on the

following negative going edge b) Active low clock: Data are clocked in on negative-going edge of clock pulse and transferred to output on the following positive going edge.

The logic diagram of J-K Master-Slave flip-flop is shown in the figure 14

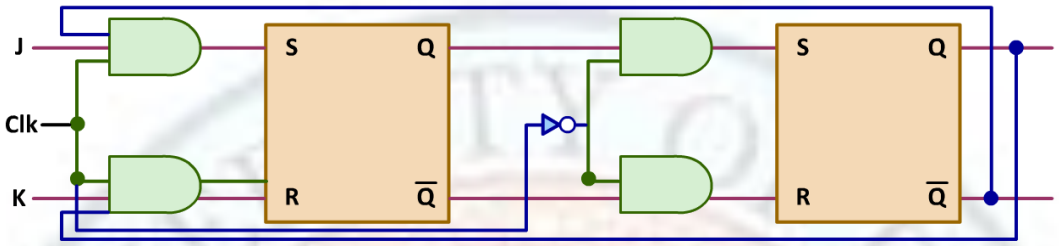

Figure 14: Circuit diagram of J-K Master-Slave flip-flop

It can be seen from the diagram that it is composed of two sections namely master section and the slave section. The slave section is replica of master section, the only difference is that slave is clocked on the inverted clock pulse and is controlled by the outputs of the master section rather than by external J-K inputs. When the clock is high, Master responds to its J and K input and slave remains inactive.

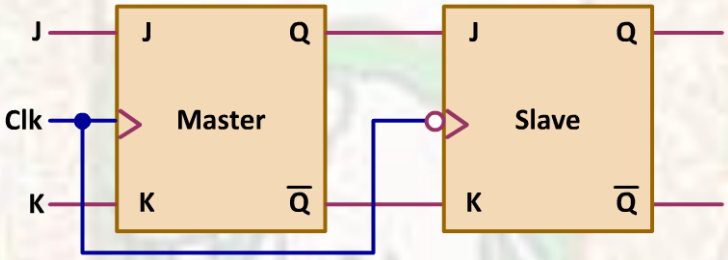

Figure 15: Block diagram of J-K Master-Slave flip-flop

Circuit Operation:

If J=1 and K=0, the master sets when the clock is high. The high output Q=1 of the master drives the J input of the slave. When the clock becomes low the slave sets, copying the action of master. If J=0 and K=1, the master resets when the clock is high. The output $\overline{Q}$ of master section becomes high which drives the K input of the slave section. When the clock is low, slave copies the action of master and thus resets. If both J and K are high, the slave copies the master. When the clock is high and J and K inputs are high, master toggles once. As soon as the clock goes low the slave will toggle once. If the master toggles into set state, the slave copies the master and toggles into set state. If the master toggles into reset state, the slave again copies the master and toggles into reset state. J-K master slave flip-flop is popularly used as counting devices.

4.5 Asynchronous Preset and Clear Operations

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In all the flip-flops discussed so far the inputs namely S-R, D and J-K inputs are synchronous inputs as the data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse, so the data is synchronized with the clock input. But sometimes one need to RESET or SET the flip-flop instantly and by using the synchronized inputs it is not possible as they are dependent of clock pulse. Most integrated circuit flip-flops have asynchronous inputs. Asynchronous inputs are the one which changes the flip-flop output immediately without even bothering about the clock pulse, so these inputs affect the state of the flip-flop independent of the clock. They are labeled as PRESET (PR) and CLEAR (CLR) in many digital systems. An active PRESET will SET the flip-flop and an active CLEAR will reset the flip-flop irrespective of the clock input. Figure 16 shows the D flip-flop where both inputs are included.

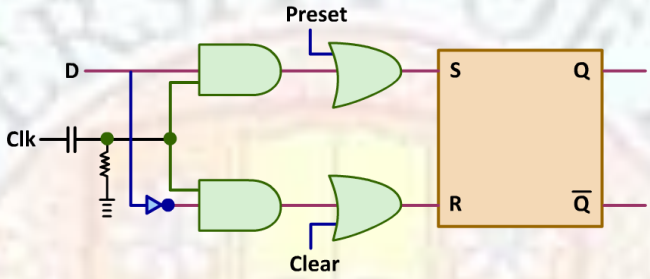

Figure 16: Circuit diagram of D flip-flop with asynchronous inputs

The circuit diagram of D flip-flop is exactly the same as given in figure 6 except the inclusion of two OR gates with PRESET and CLEAR inputs. It can be clearly verified that a high PRESET will set the flip-flop and forces the output Q=1 and high CLEAR will reset the flip-flop which forces the output Q=0 irrespective of the clock input or even the data input. Figure 17 (a) shows the logic symbol of D flip-flop with PRESET and CLEAR inputs when active high and figure 17 (b) shows the logic symbol of D flip-flop with PRESET and CLEAR inputs when active low. An active low level at the PRESET input will SET the flip-flop and active low level at the CLEAR input will reset it.

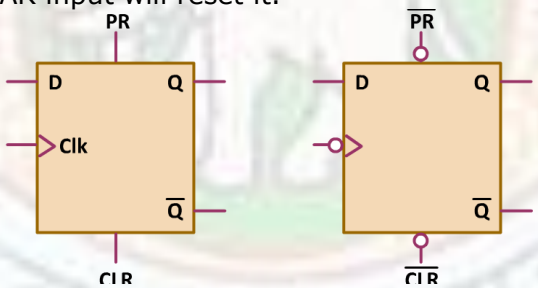

Figure 17 a) Logic symbol of D flip-flop with active high PR and CLR input b) Logic symbol of D flip-flop with active Low PR and CLR input

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Value Addition

Signal Edges

In electronics, a signal edge is a transition in a digital signal either from low to high (0 to 1) or from high to low (1 to 0). It is called an "edge" because the square wave which represents a signal has edges at those points.

A rising edge is the transition from low to high. It is also named positive edge. When a circuit is rising edge-triggered, it becomes active when its clock signal goes from low to high, and ignores the high-to-low transition.

A falling edge is the high to low transition. It is also known as the negative edge. When a circuit is falling edge-triggered, it becomes active when the clock signal goes from high to low, and ignores the low-to-high transition.

A leading edge is an event that is triggered on the front edge of a pulse. Assuming a clock begins at t = 0, the first position would be triggered at t = 1.

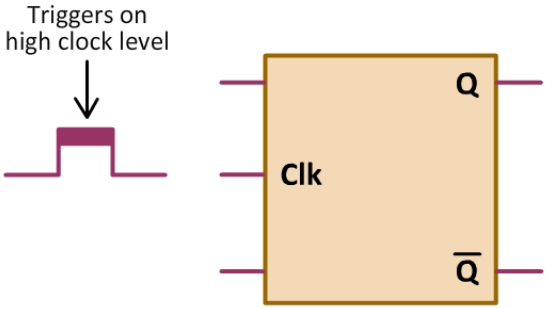
A trailing edge is the opposite of a leading edge. It is triggered on the back edge of a pulse. Assuming the clock begins at t = 0, the first position would be triggered at t = 0.

The terms front edge or leading edge, and back edge or trailing edge describe the related position of edges in a clock cycle. A leading edge can be a falling edge.

In the case of Flip Flops, the change in signal level decides the type of trigger that is to be given to the input. There are mainly four types of pulse-triggering methods. They differ in the manner in which the electronic circuits respond to the pulse. They are

1. High Level Triggering

A flip-flop responds to the clock pulse when it is in high state. The following figure depicts high level triggering



High Level Triggering

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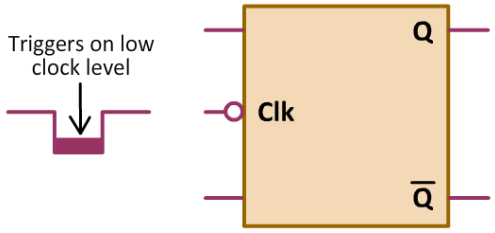
2. Low Level Triggering

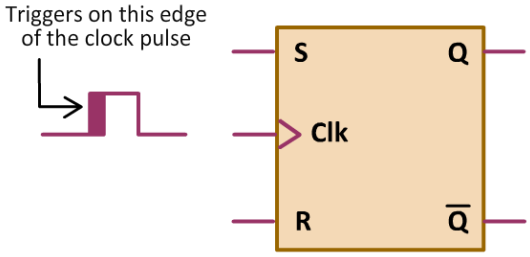
A flip-flop responds to the clock pulse when it is in low state. It is identified from the clock input lead along with a bubble. The following figure depicts low level triggering



Low Level Triggering

3. Positive Edge Triggering

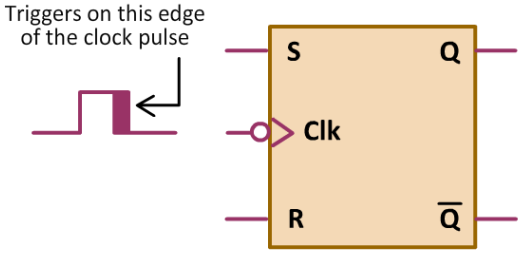
A flip flop becomes active when its clock signal goes from low to high, and ignores the high-to-low transition. In the logic symbol it can be identified from the clock input lead along with a triangle. The following figure depicts positive edge triggering



Positive Edge Triggering

4. Negative Edge Triggering

A flip flop becomes active when the clock signal goes from high to low, and ignores the low-to-high transition. In the logic symbol it can be identified from the clock input lead along with a low-state indicator and a triangle. The following figure depicts negative edge triggering



Negative Edge Triggering

Source: http://en.wikipedia.org/wiki/Signal_edge

4.6 Flip-flop operating characteristics

Propagation delay time

In analog electronics, even a simple diode a transistor takes a small amount of time for activation. A diode takes time to on or off and transistor takes time to switch states. This switching time is the main cause of delay. Such a propagation delay is also present in digital systems. The propagation delay time t_p is the amount of time it takes for the output of a gate or flip-flop to change states after the input changes. If t_p=20 ns then it takes 20 ns for the output to change after the input data has sampled by the clock edge.

Set-up time

The setup time t_s is the minimum time for which the data input levels need to be maintained constant on the input terminals of the flip-flop, prior to the arrival of the triggering edge of the clock pulse. If t_s=20 ns, the data input must be present 20 ns before the clock edge arrives.

Hold time

The hold time t_h is the minimum time for which the data input level must be maintained constant at the input terminal of the flip-flop after the arrival of the triggering edge of the clock pulse. If t_s=20 ns and t_h = 10 ns, the data bit must be present at the input terminal at least 20 ns before the clock edge arrives and held at least 10 ns after the clock edge hits. Figure 18 clearly shows all three operating characteristics.

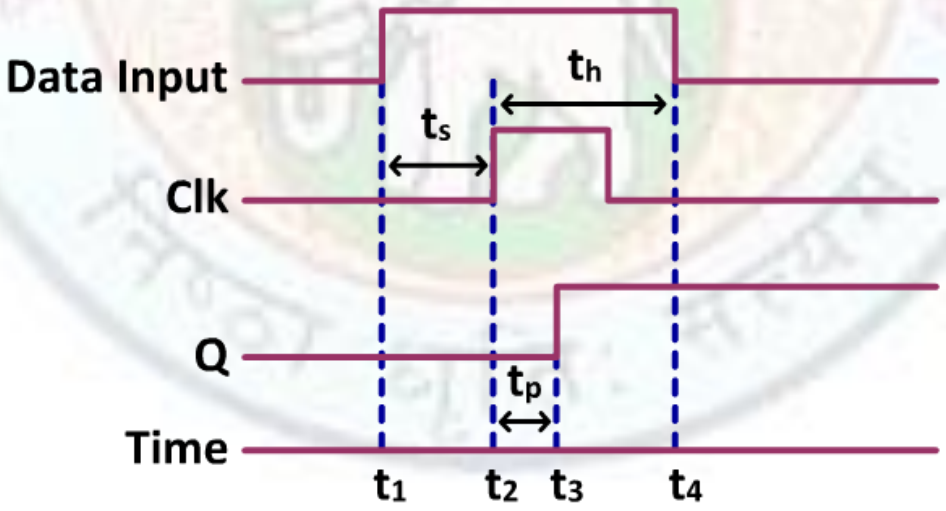


Figure 18 Operating characteristics of flip-flop

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Application of flip-flops

Flip flops are used in digital electronics some of its main applications are described below.

Shift registers

In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the "bit array" stored in it, shifting in the data present at its input and shifting out the last bit in the array, at each transition of the clock input.

More generally, a shift register may be multidimensional, such that its "data in" and stage outputs are themselves bit arrays: this is implemented simply by running several shift registers of the same bit-length in parallel.

Counter

In digital logic and computing, a counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. In electronics, counters can be implemented quite easily using register-type circuits such as the flip-flop

Frequency Division

Flip flops can divide the frequency of periodic waveform. When a pulse wave is used to toggle a flip flop, the output frequency becomes one half the input frequency. The output of each flip flop is half the frequency of an input. An arrangement of flip flops is a classic method for integer-n division. Such division is frequency and phase coherent to the source over environmental variations including temperature. The easiest configuration is a series where each flip-flop is a divide-by-2. For a series of three of these, such system would be a divide-by-8. By adding additional logic gates to the chain of flip flops, other division ratios can be obtained. Integrated circuit logic families can provide a single chip solution for some common division ratios.

If the input frequency is 80 KHz then output frequency of each flip flop would be 40 kHz for first flip flop, 20 kHz after second flip flop and 10 kHz after third flip flop.

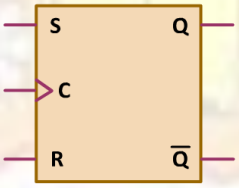
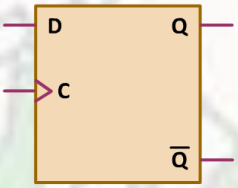
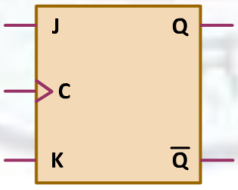
http://en.wikipedia.org/wiki/Frequency_divider

http://en.wikipedia.org/wiki/Counter

http://en.wikipedia.org/wiki/Shift_register

4.7 Summary

- Edge triggered flip-flops are bistable devices with synchronous inputs whose state depends on the inputs only at the triggering transition of a clock pulse. changes in the outputs occur at the triggering transition of the clock.
- Pulse-triggered master-slave flip-flops are bistable devices with synchronous inputs whose state depend on the inputs at the leading edge of the clock pulse, but whose output is postponed and does not reflect the internal state until the trailing edge of the clock pulse. The synchronous inputs should not be allowed to change while the clock is HIGH.
- Symbols and truth table for edge triggered flip-flops are summarized below:

Edge triggered Flip-flop	Logic Symbol	Truth Table
Positive edge triggered S-R Flip-flop		**CLK** | **S** | **R** | **Q_{n+1}** 0 | X | X | Q_n ↑ | 0 | 0 | Q_n ↑ | 0 | 1 | 0 ↑ | 1 | 0 | 1 ↑ | 1 | 1 | ?
Positive edge triggered D Flip-flop		**CLK** | **D** | **Q_{n+1}** 0 | X | Q_n ↑ | 0 | 0 ↑ | 1 | 1 ↓ | X | Q_n
Positive edge triggered J-K Flip-flop		**CLK** | **J** | **K** | **Q_{n+1}** 0 | X | X | Q_n ↑ | 0 | 0 | Q_n ↑ | 0 | 1 | 0 ↑ | 1 | 0 | 1 ↑ | 1 | 1 | $\overline{Q_n}$

- Asynchronous inputs changes the flip-flop output immediately independent of the clock pulse, Preset and Clear are examples of Asynchronous inputs.

- The propagation delay time t_p is the time it takes for the output of a gate or flip-flop to change states after the input changes.
- The setup time t_s is the minimum time for which the data input levels need to be maintained constant on the input terminals of the flip-flop, prior to the arrival of the triggering edge of the clock pulse.
- The hold time t_h is the minimum time for which the data input level must be maintained constant at the input terminal of the flip-flop after the arrival of the triggering edge of the clock pulse.

Sequential Circuits-II

4.8 Exercise

4.8.1 Subjective Questions

1. Distinguish between synchronous and asynchronous latch.
2. Distinguish between a gated D latch to an edge triggered D flip-flop.
3. Define toggling and race around condition.
4. Discuss the methods to avoid racing.
5. How do you convert one flip-flop to another.
6. Draw the binary waveform when the following input are given to negative edge triggered D flip-flop.

7. Give the fundamental difference between pulse edge triggered and edge triggered flip-flop.
8. If D input of D flip-flop changes from low to high in the middle of the positive going clock edge
   (1) Describe what happens if the flip-flop is positive edge triggered
   (2) Describe what happens if the flip-flop is a Master-Slave flip-flop.

4.8.2 Multiple Choice Questions

1) The PRESET and CLEAR inputs are

A) Synchronous inputs	B) Asynchronous inputs
C) Clock input	D) None of the above

2) Race around condition can be avoided by

A) Adjusting propagation delay time	B) Using edge-triggered flip-flop
C) Using Master-Slave flip-flop	D) All of the above

3) If both synchronous and asynchronous inputs on a J-K flip-flop are activated which input will control the output

A) Clock input	B) Synchronous input
C) Asynchronous input	D) both a and b

Sequential Circuits-II

4) If the clock pulse width is 10 ns then to avoid racing, the propagation delay should be

A) t_p >10 ns	B) t_p <10 ns
C) racing is impossible to avoid	D) t_p =1 ns

5) In an edge triggered D flip-flop

A) The output follows the input at clock edge.	B) The output can change its state anytime
C) works irrespective of clock	D) None of the above

6) When PR=1 in a positive edge triggered D flip-flop then

A) Output will follow D input	B) Q=1
C) Q=0	D) output changes only on the positive edge of clock

7) A positive edge triggered flip-flop changes its state on the …….. transition of clock pulse

A) High to low	B) Low to high
C) Anytime	D) None of the above

8) which of the following circuit can be used to design an edge triggered clock

A) RC Differentiator	B) RC Integrator
C) RC Amplifier	D) RC Oscillator

9) Toggling more than once during a clock pulse is known as

A) Racing	B) SET
C) RESET	D) walking

10) If t_s=30 ns and t_h=20 ns the data bit must be present at the input terminal

A) atleast 30 ns before the clock edge arrives	B) Atleast held for 20 ns after the edge hits
C) both a and b	D) At any time

11) The minimum time for which the data input level needs to be maintained constant on the input terminals of the flip-flop prior to the arrival of clock pulse is known as

A) Hold Time	B) Propagation delay time
C) Setup time	D) None of the above.

Answer to Multiple choice questions:

1) Asynchronous inputs
Justification:
Asynchronous inputs changes the flip-flop output immediately independent of the clock pulse, Preset and Clear are examples of Asynchronous inputs.

2) All of the above
Justification:
Race around condition can be avoided by Adjusting propagation delay time, Using edge-triggered flip-flop or by using Master-Slave flip-flop.

3) Asynchronous inputs
Justification: If both synchronous and asynchronous inputs on a J-K flip-flop are activated then asynchronous inputs will control the output as Asynchronous inputs are the one which changes the flip-flop output immediately without even bothering about the clock pulse.

4) $t_p > 10$ ns
Justification: If $t_p > T$, the output change approximately t_p sec after the leading edge of the clock. As the clock width is narrower than t_p sec, the returning Q and $\overline{Q}$ arrives too late to cause false triggering thus avoiding toggling more than once during a clock pulse and thereby avoids racing condition.

5) The output follows the input at clock edge.
Justification: Edge triggering is sensitive only at the transitions of the clock.

6) Q = 1
Justification: An active PRESET will SET the flip-flop and an active CLEAR will reset the flip-flop irrespective of the clock input.

7) Low to high

Justification: When there is a transition from 0 to 1 it is named as positive edge triggered and when the clock pulse makes a transition from high to low i.e. from 1 to 0 it is termed as negative edge triggered.

8) RC Differentiator
Justification: In the RC differentiator circuit, RC time constant is made much smaller that the clock pulse width. Because of very small time constant the capacitor charges immediately when the clock goes high. This exponential charging of capacitor produces a narrow positive spike across the resistor. Similarly capacitor discharges fully at the trailing edge of the clock pulse resulting in narrow negative spike.

9) Racing
Justification: Racing or race around condition means toggling more than once during a clock pulse. For example when the inputs J=K=1 and assuming that Q=0 then after the propagation delay time (t_p) taken by the gates in J-K flip-flop the output will toggle and the new output will be Q=1.

10) Both a and b
Justification: If t_s=30 ns and t_h = 20 ns, the data bit must be present at the input terminal at least 30 ns before the clock edge arrives and held at least 20 ns after the clock edge hits.

11) Setup time
Justification: The setup time t_s is the minimum time for which the data input levels need to be maintained constant on the input terminals of the flip-flop, prior to the arrival of the triggering edge of the clock pulse.

4.9 Glossary

Asynchronous Having no fixed time relationship; not occurring at the same time.

Clear An asynchronous input used to reset a flip flop i.e. to make the output 0.

Hold time The time interval required for the control levels to remain on the inputs to a flip flop after the triggering edge of the clock in order to reliably activate the device.

Preset An asynchronous input used to set a flip flop i.e. to make the output 1.

Propagation delay time The time interval between the occurrence of an input transition and the occurrence of the corresponding output transition in a logic circuit.

Set-up time The time interval required for the control levels to be on the inputs to a flip-flop prior to the triggering edge of the clock.

Trigger A pulse used to initiate a change in the state of the logic circuit.

4.10 Reference Books:

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