Digital Electronics

Lesson: Timers (Use Black Box approach):- 555 Timer and its Applications: Astable and Monostable Multivibrator

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1. Introduction - Timers (Black box approach) 555 timer IC

Timers are generally described as repetitive waveform generators (popularly called clock) that are essentially used to control certain sequence of an occurrence while counting in stipulated time intervals. Timers find applications typically in fields including:

a) Microprocessors and Microcontrollers
b) Counters
c) Transducers
d) Data Acquisition
e) Starting and ending industrial processes
f) Traffic lights
g) Car Tachometer
h) Remote TV jammers
i) Sirens, light detectors, touch switches etc.

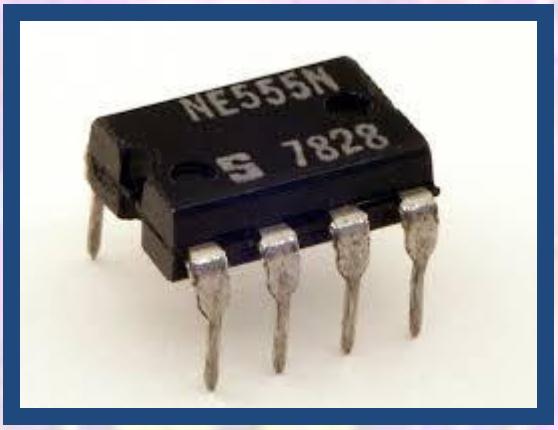

Figure 1: NE 555 timer IC

Developed by an US company Signetics and introduced worldwide in 1971, 555 is one of the most well-known timer integrated circuits (ICs) till date. It finds use in a variety of timing and oscillator applications, time delays, flip-flop element besides pulse generation. Although the manufacturing technology of 555 timer IC has matured from bipolar (original) to low-power CMOS, however it is still popular worldwide (more than a billion units are sold annually) simply because of its low price, ease of use, and stability.

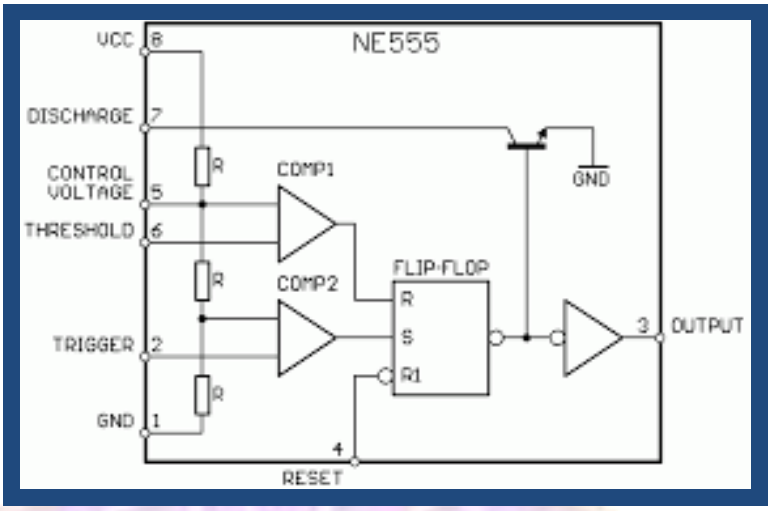

Figure 2: Basic connection details within 555 timer IC

555 IC is essentially a timer that can be configured to produce a simple pulse, a continuous rectangular wave (that can be modified to a square waveform) or a triangular / sawtooth wave (modified from capacitor charging and discharging). The type of signals that would be generated by the 555 timer IC is governed by the following:

a) The kind of electronic components connected externally to the 555 IC

b) The means how the electronic components are connected externally to the 555 IC

2. Internal components of 555 timer

The 555 timer IC has essentially five kinds of internal components that govern its functioning and the same are listed as here-under

i) Voltage divider

ii) Comparator

iii) R-S Flipflop

iv) Transistor (Bipolar Junction Transistor)

v) Out buffer

2.1 Voltage divider

Internally 555 IC consists of three resistors (each of 5 KΩ). The function of these three resistors is to from a voltage divider that applies two-thirds of the power supply voltage (Vcc) to the inverting input terminal of upper comparator (COMP 1) while applying one-third of Vcc to the non-inverting terminal of the lower comparator (COMP 2) as shown in Figure 2.

2.2 Comparator

Two voltage comparators upper (COMP 1) and lower (COMP 2) are inside the 555 timer IC. The connections of the two comparators to the voltage divider ensures the following:

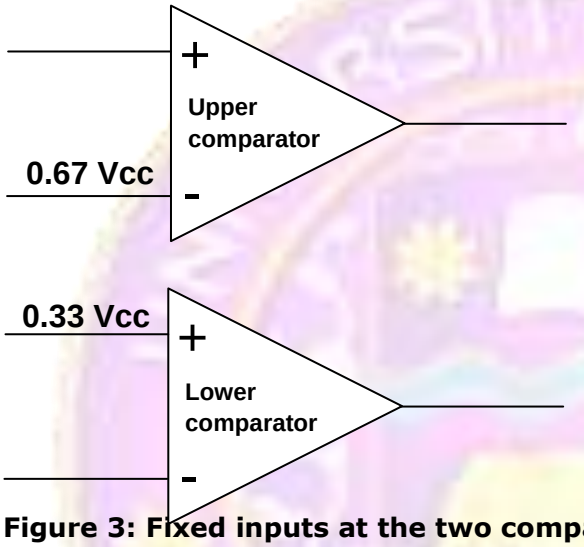

Figure 3: Fixed inputs at the two comparators

Comparators have a characteristic that whenever input voltage at their non-inverting input is greater in magnitude than on its inverting input then their outputs produce positive voltage. Internal conditions ensure that output from both the comparators can never be a positive voltage at the same time, however they can be zero.

2.3 R-S flip flop

The output of the upper comparator (COMP 1) is connected to the R input of the flip-flop while output of the lower comparator (COMP 2) is connected to its S input. Flip flops are digital 'electronic component' that typically have two inputs (R & S) and two outputs (Q and Q'). One out is ALWAYS complement state of the other. Complement refers to the fact if one is logic HIGH then its complement would be logic LOW. The inputs and outputs of the flip flop are either logic HIGH or logic LOW and nothing in between. Logic High and logic LOW are preset voltages and generally logic LOW is zero volts (0 V), while logic HIGH is typically +5 V. The output of the RS flip flop is summarized in the following truth table

R input	S input	Q output
0	**0**	**Last state**
0	**1**	**0**
1	**0**	**1**
1	**1**	**NOT ALLOWED**

It is interesting to note that since output from both the comparators can never be positive (HIGH) voltage simultaneously hence the condition of R = 1 = S would never occur.

Also complement of the output of the RS flip flop is connected to the output buffer besides the base of the NPN bipolar junction transistor (BJT).

2.4 NPN bipolar junction transistor (BJT)

The NPN bipolar junction transistor (BJT) acts as a switch and its main function is to act as a path of discharge. The NPN BJT conducts current between its emitter and collector whenever a positive voltage is present at its base. Likewise it stops the flow of current between the emitter and collector whenever the base has zero voltage.

2.5 Output buffer

The job of the output buffer is to produce high current and voltage so as to be able to produce sufficient power in the 555 IC to drive external devices / circuitry. Figure 2 shows that output buffer receives its input from the complement voltage output of the RS flip flop.

3. Basic working of 555 timer

555 timer IC (Figure 2) is thus mainly seen to consist of three 5 KΩ resistors (hence the name 555) constituting a voltage divider, two voltage comparators, flip-flop and transistors for discharge. Inside the IC the 5 KΩ resistors are connected in series with the DC power supply (Vcc). The 555 timer IC functions in a stable manner within the DC supply range of 5 – 15 V while 18 V is the absolute maximum. Within the 555 timer IC, the lower voltage comparator (COMP 2) has 1/3 Vcc supply voltage applied to its positive input terminal while 2/3 Vcc voltage is applied to the negative terminal of the upper comparator (COMP 1). It is advisable to connect 555 timer ICs to 6V, 9V or 12V (Vcc

values) because of its operation between 2/3 and 1/3 Vcc and hence ease of plotting on CROs.

SUPPLEMENTARY READING

Operational amplifiers (op-amps) and a special class of differential amplifiers which possess a balanced difference input with a very high gain and most voltage comparators are based on them. Typically low performance (cheap) voltage comparators are realized by using a standard op-amp (741C) operating in open-loop configuration (without negative feedback). Whenever, non-inverting input (V_+) has a higher voltage input than its inverting input counterpart (V_-), the high open-loop gain of the op-amp causes its output to saturate at the highest positive voltage the op-amp IC can output. On the contrary whenever non-inverting input (V_+) drops below the inverting input (V_-), the output saturates at the most negative voltage it can output. The op-amp's output voltage is limited by the supply voltage.

In the 555 timer IC whenever the voltage at the trigger terminal (TRIGGER) falls below 1/3 Vcc, the set (S) terminal of the flip-flop (FF) attains a high level and the FF is said to be set. Likewise whenever the voltage of at the threshold terminal (THRESHOLD) becomes higher than 2/3 Vcc, the reset (R) terminal of the FF attains a high level and the FF is considered to be reset. The output of the 555 timer IC exhibits various patterns as it oscillates between 2/3 Vcc and 1/3 Vcc

SUPPLEMENTARY READING

Flipflops (FFs) are bistable binary circuits that act as the basic memory element in digital electronics. The FFs change their state (from 0 to 1 and vice-versa) when signals are applied to its one or more control inputs and which influence their one or two outputs.

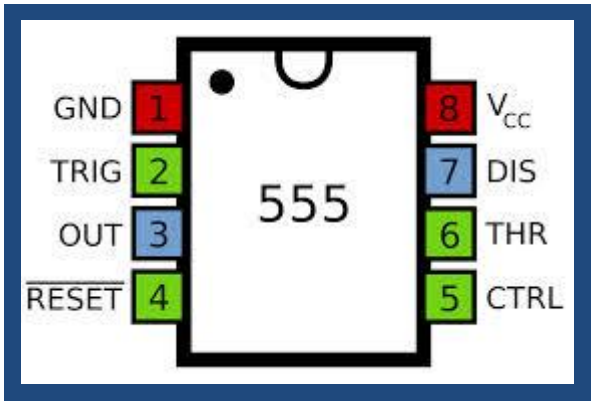

Figure 4: Pin-out diagram of 555 timer IC

4. Description of various pin terminals of 555 timer

Figure 4 shows the pin-out diagram of 555 timer IC which is typically available as a 8 – pin dual-in-line package (DIP). Pin #1 (0 V) and pin #8 (+ 5 to +15 V) are used to connect DC power supply (5 – 15 V).

Pin #2 is TRIGGER, in monostable configuration of 555 timer, initiates a high to low transition and otherwise whenever voltage at this pin falls below 1/3 Vcc triggers the timer.

Pin #3 is the OUTPUT pin which exhibits a rectangular or square wave (astable operation) or a high value for a predetermined set time (monostable operation).

Pin #4 is the RESET which if NOT used is connected to Vcc.

Pin #5 is CONTROL VOLTAGE, 555 timer manufacturer states that for reliable operation a 0.01 µF capacitor needs to be connected between this and the circuit ground.

Pin #6 is the THRESHOLD that detects whether the voltage on the timing capacitor has risen over 2/3 Vcc and resets the output whenever this takes place.

Pin #7 is the DISCHARGE and is used to provide a discharge path from the timing capacitor to ground when the output is low.

Suggested Simulation

https://www.wisc-online.com/learn/career-clusters/stem/sse7806/internal-elements-of-a-555-timer

As the name suggests a multivibrator (generator of multiple frequencies) in astable mode has no stable output. It always has an output that switches back and forth between two states and in the case of 555 IC generally a rectangular output is obtained. This rectangular output can be converted to square wave output with some minor modifications to the external circuit. Also the rate at which the output switches back and forth (frequency) between the high and low states can be accurately controlled by the end-user / designer. 555 timer IC therefore finds applications as a clock generator over a broad range of applications. Another advantage that 555 timer IC has, is the wide range of time-period (= 1/frequency) over which it can generate stable waveforms (microseconds to hours).

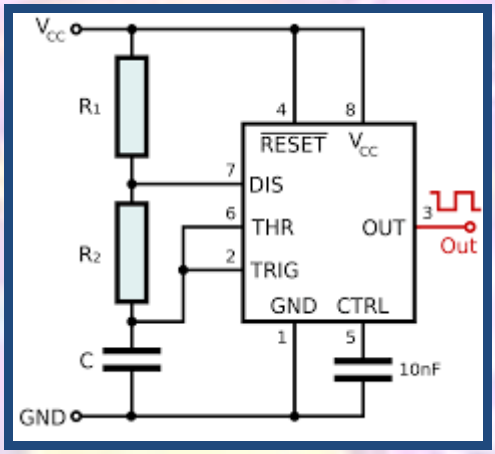

Figure 5: 555 timer IC configured in astable mode

Figure 5 shows the 555 timer IC in astable configuration mode with two external resistors R_1 and R_2 and a timing capacitor C. Manufacturer of 555 timer IC warrants that a 0.01 μF (microfarad) capacitor be affixed between its CONTROL (Pin # 5) and ground for stable operation.

As soon as the 555 timer IC is biased with Vcc (DC source) the following zero state conditions are assumed:

i) Timing capacitor C is fully discharged

ii) Output of the upper comparator (COMP 1) is LOW

iii) Output of the lower comparator (COMP 2) is HIGH

iv) Discharge BJT is switched OFF

v) RS Flip flop output is HIGH and its complemented output is LOW

vi) Output of the buffer is HIGH

As soon as the Vcc power is applied to the circuit current begins to flow through R_1, R_2 and C. The timing capacitor (C) begins to charge in an exponential fashion and the potential across the capacitor is directly connected to the inverting terminal of the lower comparator (COMP 2). As soon as the capacitor C charges beyond 0.33 Vcc the output of the lower comparator goes low. This is because the non-inverting terminal of the lower comparator is fixed at 0.33 Vcc due to connection with the 5 KΩ voltage divider. As the capacitor keeps charging towards Vcc and crosses the 0.67 Vcc threshold value then the upper comparator (COMP 1) changes its output to HIGH. As soon as this happens, R input of the flip-flop goes HIGH and its S input goes LOW. This results in the flip flop output Q going LOW and, its complement out Q' going HIGH. This change in RS flip flop output results in output buffer going LOW. Further, a HIGH Q' results in the NPN BJT switching ON and providing the timing capacitor C a path to discharge. As soon as the capacitor begins to discharge the potential across it begins to fall, leading to the upper comparator going LOW. With constant discharge when the capacitor potential falls below 0.33 Vcc the output of the lower comparator goes HIGH. With the upper comparator at LOW output and lower comparator with HIGH output again the RS flip flop changes its output (Q) to HIGH and hence its complement state Q' goes LOW. The output buffer goes HIGH while the NPN BJT gets cut-off thus blocking any more discharge of the capacitor. Hence the capacitor starts to charge once again through R_1 and R_2. The cycle starts repeating all over again. It is therefore noted that as long as power (Vcc) is provided to the astable configuration of the 555 timer IC the potential on its timing capacitor would oscillate between 0.67 Vcc and 0.33 Vcc. Only the first time the capacitor would charge from 0V to 0.67 Vcc and thereafter the oscillation would begin.

Suggested simulation

https://www.wisc-online.com/learn/technical/electronics-solid-state/sse8106/the-555-astable-multivibrator#

5.1 Timing calculations in 555 timer in astable configuration

The charging of the timing capacitor happens through R_1 and R_2 and hence the time for which one obtains a HIGH value at the output (Pin # 3) of the 555 timer IC is given by

$T_{HIGH} = 0.693 (R_1 + R_2) C$ seconds [since RC = time constant]

The discharge of the capacitor takes place only through the resistor R_2 and hence the time for which one obtains a LOW value at the output (Pin # 3) of the 555 timer IC is given by

$T_{LOW} = 0.693\ (R_2)\ C$ seconds

Activity

Take a dual-trace CRO/DSO and fix up its two vertical channel probes at Pin # 2 and Pin # 3 of a 555 timer IC configured in astable mode. Plot the waveforms thus obtained.

5.2 Waveforms obtained during the above activity

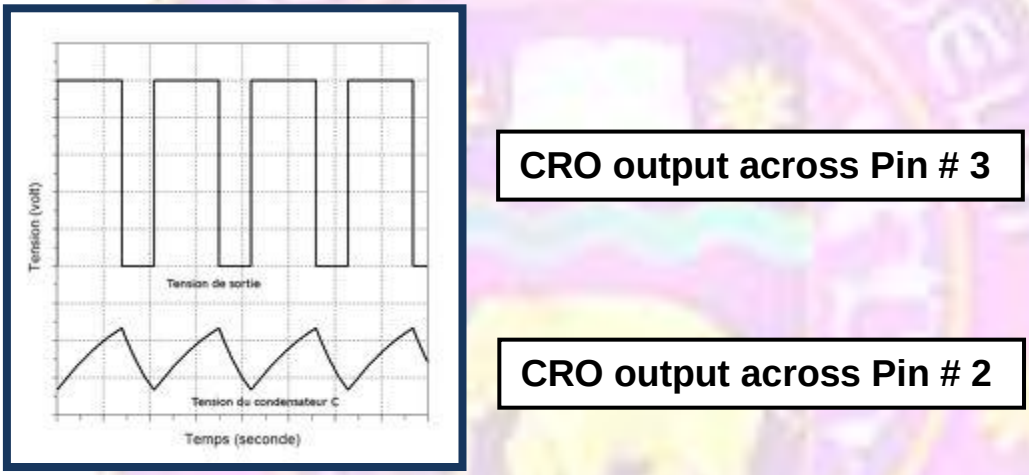

Figure 6: Waveforms obtained on a dual-trace CRO/DSO at Pin # 3 and Pin # 2 of a 555 timer IC configured in astable mode

Important Tip

Whenever NO output is obtained at Pin # 3 of the 555 timer IC it is prudent to check whether the timing capacitor is charging and discharging properly i.e. a saw-tooth wave is being obtained across it.

Duty cycle (%) of the waveform is defined as

$$D = T_{HIGH} / (T_{HIGH} + T_{LOW}) \times 100$$

It is important to note in 555 time IC configured in astable mode, that the timing capacitor (C) would always charge through R_1 and R_2 but discharge through R_2 only. Hence the output waveform normally would always be rectangular in nature with HIGH time being larger than the LOW time.

50% DUTY CYCLE (Square wave output)

In order to obtain a square wave output from 555 timer in astable mode, one has to somehow realize $\mathbf{T_{HIGH} = T_{LOW}}$ (50% Duty Cycle)

The easiest option seen is to put R_1 = 0Ω, however it is NOT feasible as it would wreck the stability and integrity of the 555 timer as astable multivibrator. Also having same resistance values for R_1 and R_2 (i.e. $R_1 = R_2$) does NOT solve the problem.

PRACTICAL SOLUTION TO OBTAIN 50% DUTY CYCLE

The practical solution to obtain 50% duty cycle is to use a diode across the R_2 resistor while keeping the values of the resistors R_1 and R_2 same.

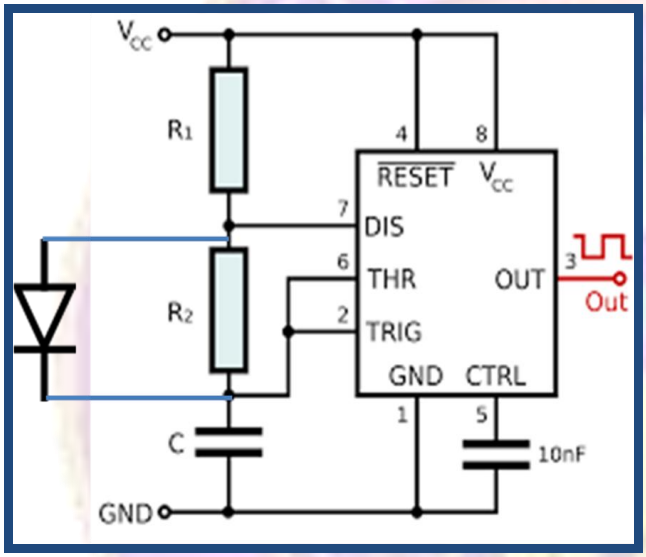

Figure 7: 555 timer IC in astable mode configured as a square wave generator

Figure 7 shows the 555 timer IC in astable mode configured as a square wave generator. It is pertinent to note that with values of both the resistors kept equal ($R_1 = R_2$) during charging, the current passes through R_1 but bypasses R_2 since the affixed diode being forward biased offers an easier path for it (ideal diode in forward bias offers zero resistance). During discharge of the capacitor only R_2 resistance comes into play since during this time the current cannot flow through the diode since it is reverse biased and offers a very high resistance.

6. 555 timer IC in Monostable mode (single shot / one shot)

As the name suggests monostable multivibrator (also known as one / single shot) has one stable state and it switches to its unstable state for a predetermined time period T when it is triggered. The time period (T) is pre-determined by the external resistor (R) and timing capacitor (C) whence the RC gives the time constant. in the circuit. The main

application of the 555 timer IC in monostable mode is for generation of Pulse Width Modulated (PWM) waves and measurement of single events during data logging.

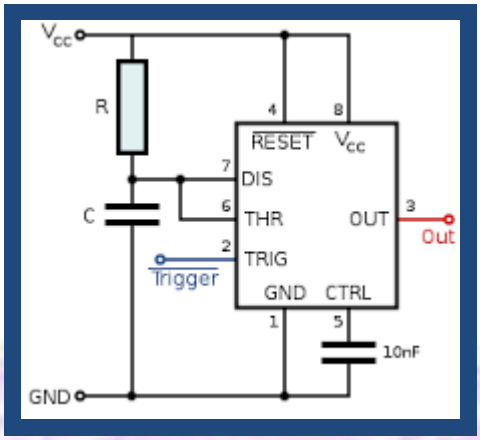

Figure 8: 555 timer IC configured in monostable mode

Figure 8 shows the 555 timer IC configured in monostable or single shot mode. It remains in its default low output state (stable state) until it is triggered. When a negative trigger (a negative going pulse) is applied to the TRIGGER (Pin # 2) of 555 Timer, the lower comparator (COMP 2) output goes HIGH and output of upper comparator (COMP1) goes LOW. HIGH output of the lower comparator makes the S input of the RS flip flop HIGH and R input LOW (since upper comparator output is R input). This makes the RS flip flop output (Q) HIGH and its complement output Q' LOW. Since Q' is connected to the base of the NPN BJT hence the discharge transistor turns OFF and the timing capacitor starts charging to Vcc (DC power supply) via the resistor R. It is assumed that the initial voltage on the timing capacitor is zero. After the negative pulse (trigger) which is momentary output of lower comparator (COMP 2) reverts to its LOW value and the upper comparator also remains LOW. This condition ensures that both the R and S inputs of the RS flip flop get fixed to LOW values and hence output does NOT change (Truth table of RS flip flop). The typical output characteristics of the 555 timer IC in monostable configuration are shown in Figure 9.

6.1 Timing calculations in 555 timer in monostable configuration

The time (t_p) during which the output of a monostable 555 timer remains high as shown in Figure 8 is given by

t_p = 1.1 RC (seconds)

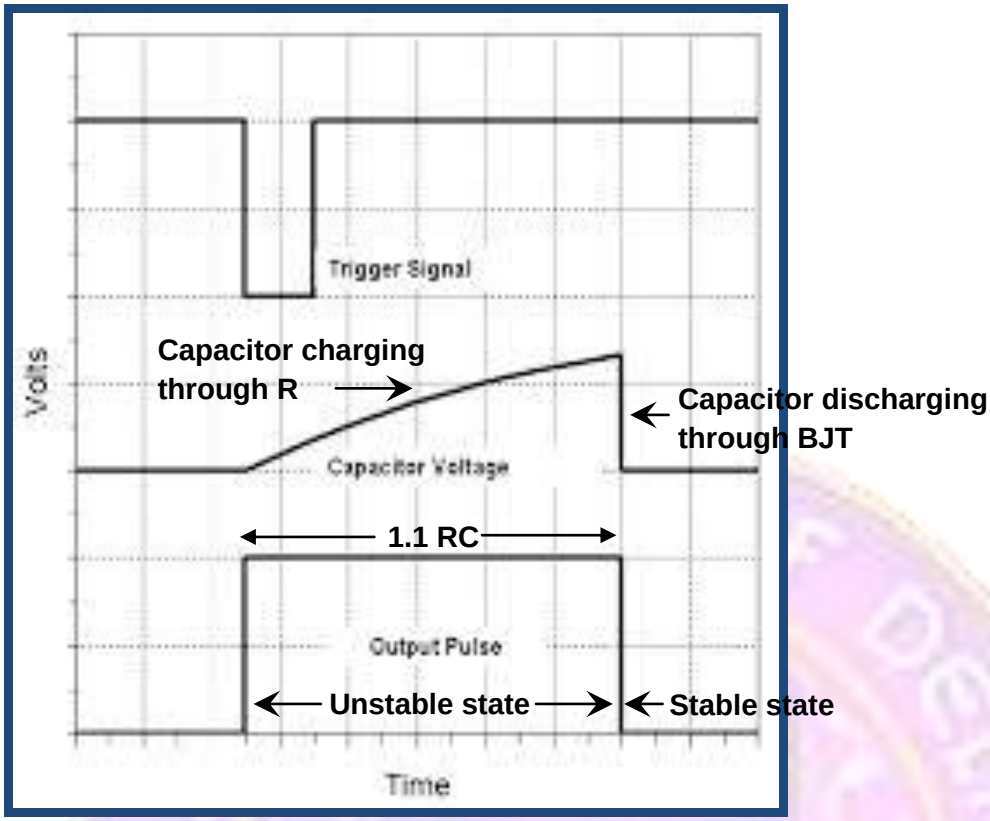

Figure 9: Typical output characteristics of the 555 timer IC in monostable configuration

ACTIVITY

How to realize 555 timer IC in monostable mode without using a CRO

In the 555 timer IC configured as a monostable multivibrator connect a Light Emitting Diode (LED) having a 100 Ω resistor in series between its output (Pin # 3) and ground. Choose the resistor (R) and timing capacitor (C) in such a way

Precaution

When choosing large capacitor values it is seen that most of them are electrolytic in nature. Electrolytic capacitors have polarities and one has to be careful while connecting them. An electrolytic capacitor when connected with reverse polarity beyond a particular voltage is prone to explode.

6.2 How to apply trigger to 555 timer IC in monostable mode

In order to trigger the 555 timer IC in monostable mode the TRIGGER (Pin #2) has to momentarily fall below 0.33 Vcc. The duration of the trigger pulse should be such that it must never be longer than the duration of the 555 timer output.

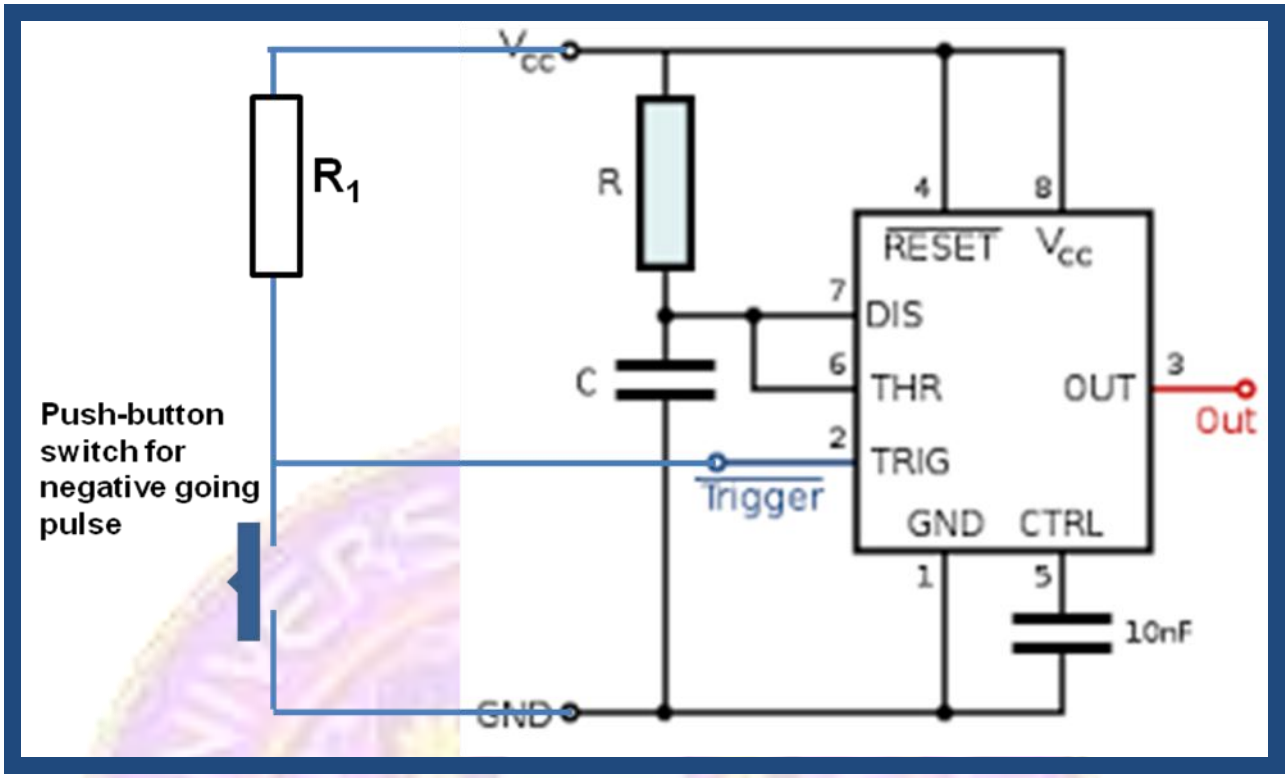

Figure 10: 555 timer IC configured in monostable mode with trigger circuit

Figure 10 shows the 555 timer IC configured in monostable mode with trigger circuit. The trigger circuit essentially consists of a resistor (R_1) connected between Vcc and TRIGGER (Pin #2). Further the TRIGGER is connected to the ground (GND) via a push-button switch. The value of resistor should be very high (> 1 MΩ) since it is used to prevent flow of high current during generation of the negative going pulse at Pin #2. This circuit for triggering is useful only for time-period in seconds. For triggering faster waveforms output of a 555 timer configured in astable mode can be used for triggering.

SUMMARY: After studying this chapter, you should be able to

- Explain and analyze the operation of 555 timer.
- Describe internal components of 555 timer and discuss their function
- Explain the function of various pins of 555 timer
- Explain working of 555 timer in Astable mode
- Explain working of 555 timer in Monostable mode
- Describe various output wave forms obtained

- Design timing circuits using 555 timer
- Understand limitations of 555 timer

EXERCISES

Question Number	Type of question
1	Multiple choice questions

1. In which decade did the 555 timer IC start being used commercially
(a) 1950 (b) 1970 (c) 1990 (d) 2010

2. Main use of the 555 IC is
(a) As an amplifier (b) As a voltage divider (c) As a timer (d) All of these

3. 555 timer has three resistors each having a value
(a) 5 K Ω (b) 5 M Ω (c) 5 Ω (d) None of these

4. In a 555 timer in astable mode, a square wave output can be achieved by
(a) using a diode across R_A (b) $R_A = 0$ Ω (c) $R_B = 0$ Ω (d) using a diode across R_B

5. Which configuration of 555 timer is not possible
(a) Astable (b) Bistable (c) Unstable (d) Monostable

6. The function of Pin 3 is:

a) Control Voltage b) Discharge c) Output d) Reset e) Threshold g) Trigger

7. The function of Pin 6 is:

a) Control Voltage b) Discharge c) Output d) Reset e) Threshold g) Trigger

8. The function of Pin 5 is:

a) Control Voltage b) Discharge c) Output d) Reset e) Threshold g) Trigger

9. The function of Pin 4 is:

a) Control Voltage b) Discharge c) Output d) Reset e) Threshold g) Trigger

10. What is the function of the Threshold pin?

a) To charge the capacitor "C"

b) To discharge the capacitor "C"

c) To detect when the capacitor is "HIGH"

d) To detect when the capacitor is "LOW"

11. What is the function of the Discharge pin?

a) To charge the capacitor "C"

b) To discharge capacitor "C"

14. The Discharge and Output are:

a) In phase with each other

b) 90 degree out of phase with each other

c) 180 degree out of phase with each other

d) None of these

15. What does pin 6 do?

a) Charges the capacitor "C"

b) Discharges the capacitor "C"

c) Detects the HIGH on capacitor "C"

d) Detects the LOW on capacitor "C"

16. What does pin 2 do?

a) Charges the capacitor "C"

b) Discharges the capacitor "C"

c) Detects the HIGH on capacitor "C"

d) Detects the LOW on capacitor "C"

KEY

(1) b	(2) c	(3) a	(4) d	(5) c
(6) c	(7) e	(8) a	(9) d	(10) c
(11) b	(12) d	(13) b	(14) a	(15) c
(16) d				

Question Number	Type of question
2	Subjective questions

1. Describe the working of a basic 555 timer IC

2. Describe the working of 555 timer in astable configuration

3. Explain in detail how would you obtain a square wave output in 555 timer in astable mode?

4. Describe the working of 555 timer in monostable configuration

5. Describe how can you obtain output from 555 timer in monostable configuration without using a cathode ray oscilloscope?

Question Number	Type of question
3	Numericals

1. In a 555 timer in monostable mode, if R = 5 KΩ and time for which output is high is = 10 ms then determine the value of C (Ans: 1 μF)

2. For a 555 timer in astable configuration if R_a = 2.2 KΩ and R_b = 3.9 KΩ and C = 0.1 μF then determine a) the positive pulse width b) the negative pulse width and c) free running frequency f_o (Ans: a) 0.421 ms, b) 0.269 ms and c) f_o = 1.45 KHz)

3. What is the pulse width for a 555 timer based monostable circuit with R = 2.2 KΩ and C = 0.01 μF? (Ans: 24.2 μs)

4. What is the frequency and duty cycle for a 555 timer based astable circuit with R_a = 2.2 KΩ, R_b = 4.7 KΩ and C = 0.022 μF? (Ans: 5.64 KHz and 59.5%)