## Sequential Circuits-I

## Lesson: Sequential Circuits-I <br> Lesson Developer: Dr. Divya Haridas <br> College/ Department: Keshav Mahavidyalaya, University of Delhi

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## Sequential Circuits

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## Sequential Circuits-I

### 3.1 Chapters Objective

- Introduction to sequential circuits.
- Classification of sequential circuits as synchronous and asynchronous circuits.
- To design basic latches.
- To study the difference between a latch and a flip-flop.
- To design various latches.
- To design and study S-R, D and J-K Flip-flop.
- To study the mode of operation of all flip-flops.
- To interpret flip-flop waveform diagrams to determine the mode of operation.


### 3.2 Introduction

We have already studied about combinational logic circuits where the output at any instant of time depends only on the present value of the inputs, but there are many applications where the output at any instant of time depends not only on the present value of the inputs but also on past outputs. Such devices are classified as sequential circuits. Sequential circuits are those logic circuits which require both the timing and the memory device. Basically sequential logic circuit is a combination of combinational logic circuits and memory element.

The storage/memory element is connected in a feedback path to the combinational circuit. The binary information stored in these memory element at any time defines the state of the sequential circuit at that time. Logic gates are the basic building block of combinational logic circuits and flip-flop (FF) is the basic building block of sequential circuit. A flip-flop, is a kind of bistable multivibrator, which has two stable state. It remains in either of the states indefinitely till triggered by a signal to change its state. This chapter introduces you to sequential circuits, types of sequential circuits, latches and several types of flip-flop circuits.

### 3.3 Comparison between combinational circuits and sequential circuits

> In Combinational circuits, the output is dependent on the present input only and in sequential circuits the output is dependent not only on the represent input but also on the past history of the inputs.
> In combinational circuit no memory element is present whereas in sequential circuit there is at least one memory element.
> Combinational circuits are faster in terms of speed as the only delay is the propagation delay of all the logic gates used in the circuit, whereas sequential circuits are comparatively slower as they involve the propagation delay time due to logic gates and the memory element used in the circuit.
> Combinational circuits are easier to design but require more hardware whereas the sequential circuits are harder to design but require lesser hardware.

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### 3.4 Sequential Circuits

### 3.4.1 Types of sequential circuits

The sequential circuits can be classified in two ways depending on the timing of the signal, which are given as

- Asynchronous sequential circuits
- Synchronous sequential circuits

In Asynchronous sequential circuits the output of the logic circuit can change state at any time, as soon as any input changes its state whereas in the case of synchronous systems a signal namely clock signal is used to determine/control the exact time at which any output can change its state. These are also called as clocked sequential circuits. Flip-flop are the memory elements which are used in both the cases and are capable of storing 1-bit binary information. The block diagram of sequential logic circuits is shown in figure 1.


Figure1: Block diagram of sequential circuits.

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## Historical Background

The first electronic flip-flop was invented in 1919 by William Eccles and F. W. Jordan. It was initially called the Eccles-Jordan trigger circuit and consisted of two active elements ( vacuum tubes). The name flip-flop was later derived from the sound produced on a speaker connected with one of the backcoupled amplifiers output during the trigger process within the circuit. In September 1919 Eccles and Jordan described the flip-flop in a brief one-page paper, "A trigger relay utilizing three-electrode thermionic vacuum tubes," The Electrician, vol. 83, (September 19, 1919) p. 298. However, the patent, filed the previous year, and consisting of 5 pages, remains the first description of this invention.

William Henry Eccles FRS (23 August 1875-29 April 1966) was a British physicist and a pioneer in the development of radio communication. He was born in Barrow-inFurness, Lancashire, England. Eccles invented the term Diode to describe an evacuated glass tube containing two electrodes; an anode and a cathode. Following World War I Eccles' main interest was in electronic circuit development. In 1918 he worked in collaboration with F. W. Jordan to patent the flip-flop circuit, which became the basis of electronic memory in computers. In 1919, Eccles became vice-chairman of the Imperial Wireless Committee. He helped in the design of the first long wave radio station, and became involved in the early work of the British Broadcasting Company (later the BBC) following its establishment in 1922.

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Frank Wilfred Jordan was born in 1882 in Canterbury, Kent, England, the son of Edward James Jordan and Eliza Edith. In 1912 he was a "lecturer in physics", presumably at the Royal College of Science. In 1918 he was an "electrician" at City and Guilds Technical College.

This flip-flop circuit became perhaps the most important circuits in computer technology allowing memory to be stored.


Flip-flop schematics from the Eccles and Jordan patent filed 1918, one drawn as a cascade of amplifiers with a positive feedback path, and the other as a symmetric crosscoupled pair

Source: http://en.wikipedia.org/wiki/Flip-flop_(electronics)\#cite_note-3 http://en.wikipedia.org/wiki/William_Eccles http://en.wikipedia.org/wiki/F._W._Jordan http://en.wikiversity.org/wiki/EE_Digital_Electronics/Lecture_Flip-flops

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### 3.5 Latch and Flip-Flop

The latch is a bistable device which is used as temporary storage device and has two stable states. Latches are very similar to flip-flops as they too have two stable states. Also as in the case of flip-flops there is a feedback arrangement in which the outputs are connected back to the opposite inputs. The basic difference between the two is the method used for changing their state. A latch checks all its inputs continuously and the output changes immediately as there is a change in the input. In the case of flip-flop it samples its inputs and changes its output only at a time as determined by a clock signal. Thus latches are used in asynchronous sequential logic circuits and flip-flops are used in synchronous sequential logic circuits.

## Do You Know

Early flip-flops were known variously as trigger circuits or multivibrators. Prior to the invention of electronic computing Eccles and Jordan viewed their invention as a "method of relaying or magnifying in electrical circuits for use in telegraphy and telephony." However, a flip-flop circuit has two stable states and, as Claude Shannon pointed out in his Mathematical Theory of Communication (1948), a flip-flop can be used to store one bit of information. Flip-flop circuits operate using Boolean algebra (AND, OR, NOT). Thus, with the invention of electronic computing using vacuum tubes as switches, flip-flops became the basic storage element in sequential logic used in digital circuitry, and the basis for electronic memory.

### 3.6 S-R (SET-RESET) Latch

The simplest latch is the Set-Reset latch (SR or RS Latch). This can be designed using two cross-coupled NOR gates or NAND gates. It has two inputs labeled $S$ and $R$ and two outputs Q and $\bar{Q}$. The state of the latch corresponds to value of Q (high or low) and $\bar{Q}$ is compliment of Q , so that if output $\mathrm{Q}=1$ then $\bar{Q}=0$. The name of the latch, S-R or SETRESET is derived from the names of its inputs. Figure 2 shows the logic symbol of the $\mathrm{S}-\mathrm{R}$ latch.


Figure 2: Logic symbol of S-R latch
Table 1 gives the truth table of S-R latch.

| $\mathbf{R}$ | $\mathbf{S}$ | $\mathbf{Q}$ | Remarks |
| :---: | :---: | :---: | :---: |
| 0 | 0 | Last value | No change |
| 0 | 1 | 1 | Set |
| 1 | 0 | 0 | Reset |
| 1 | 1 | $?$ | Forbidden |

Table1: Truth table of S-R Latch
Figure 3 shows the SR latch using two NOR gates. The two NOR gates are cross coupled so that the output of the first NOR gate is connected to one of the inputs of second NOR gate. By this time the student already knows that having a logic 1 at any input of a NOR gate forces its output to logic 0 immediately. Using this thumb rule lets understand the working of SR Flip-flop


Figure 3: S-R latch using NOR gates

## Circuit Operation

Let us discuss the four cases as mentioned in the truth table:

## Case 1

$\mathrm{R}=0$ and $\mathrm{S}=1$
In this case, the S input of the second NOR gate is high i.e. at logic 1 , so the output $\bar{Q}$ goes to low state i.e. to logic 0 (remember the thumb rule). Since the output $\bar{Q}$ is connected to one of the input of the first NOR gate, now both the inputs of first NOR gate are at logic 0 so the output Q turns high i.e. at logic 1 as shown in the figure 3. Therefore it can clearly be depicted that when $\mathrm{S}=1$ and $\mathrm{R}=0$ it SETs the Latch.

Case 2
$\mathrm{R}=1$ and $\mathrm{S}=0$
In this case, the $R$ input of the first NOR gate is high (at logic 1 ), so the output $Q$ goes to low state (logic 0 ). Since the output Q is connected to one of the input of the second NOR gate and since both the inputs of second NOR gate are at logic 0 so the output $\bar{Q}$ turns high (logic 1) as shown in the diagram. Therefore it can clearly be depicted that when $\mathrm{R}=1$ and $\mathrm{S}=0$ it RESETs the Latch.

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Case 3
$\mathrm{R}=0$ and $\mathrm{S}=0$
Whenever such a situation arises the output retains its last value. Lets understand this concept by two examples:

1) let us assume that initially $Q=1$ and $\bar{Q}=0$. $\bar{Q}$ is connected to first NOR gate so both the inputs of first NOR gate are 0 which forces the output $\mathrm{Q}=1$. This Q is connected as an input to the second NOR gate. Any logic 1 present at the input of NOR gate forces its output to be 0 . i.e. $\bar{Q}=0$. Thus the output retains the last value and observes no change at the output.
2) Let us assume that initially $\mathrm{Q}=0$ and $\bar{Q}=1 . \mathrm{Q}$ is connected as one of the input of second NOR gate so both the inputs of second NOR gate are 0 which forces the output $\bar{Q}$ $=1$. This $\bar{Q}$ is connected as an input to the first NOR gate. Any logic 1 present at the input of NOR gate forces its output to be 0 . i.e. $\mathrm{Q}=0$. Thus the output retains the last value and observes no change at the output. This can be clearly understood by this animation.

Case 4
$\mathrm{R}=1$ and $\mathrm{S}=1$
When both the inputs are logic 1, they force the outputs of both NOR gates to logic 0 i.e. $\mathrm{Q}=0$ and $\bar{Q}=0$. Since we know that Q and $\bar{Q}$ are complementary to each other and $\mathrm{Q} \neq \bar{Q}$ at any condition, such a state is known as forbidden state. Thus in normal operation such a condition must be avoided.

## Value Addition

The timing diagram in figure 4 illustrates how the active high S-R Latch responds to a particular case of $S$ and $R$ inputs, assuming that initially the latch is SET.


Figure 4: Timing diagram

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## SR Latch using NAND gates or $\bar{S} \bar{R}$ Latch

An active low SR Latch can be designed using two cross coupled NAND gates.


Figure 5: $\bar{S} \bar{R}$ Latch using NAND gates
The logic diagram of $\bar{S} \bar{R}$ Latch is given in figure 5 and the logic symbol is shown in figure 6.


Figure 6: Logic symbol of $\bar{S} \bar{R}$ Latch
The truth table in table 2 details the operation of $\bar{S} \bar{R}$ latch.

| $\bar{R}$ | $\bar{S}$ | $\mathbf{Q}$ | Remarks |
| :---: | :---: | :---: | :---: |
| 0 | 0 | $?$ | Forbidden |
| 0 | 1 | 0 | Reset |
| 1 | 0 | 1 | Set |
| 1 | 1 | Last value | No change |

Table 2: Truth table for $\bar{S} \bar{R}$ Latch

Before understanding the circuit operation students are advised to remember the thumb rule that a logic 0 at any input of a NAND gate will force its output to be at logic 1 .

## Circuit Operation

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Case 1) when $\bar{R}=0, \bar{S}=1$ then $\bar{S} \bar{R}$ latch will Reset and forces $Q=0, \bar{Q}=1$
Case 2) when $\bar{R}=1, \bar{S}=0$ then $\bar{S} \bar{R}$ latch will Set and forces $Q=1, \bar{Q}=0$
Case 3) when $\bar{R}=1, \bar{S}=1$ then $\bar{S} \bar{R}$ latch will retain its last value and No change is observed at the output

Case 4) when $\bar{R}=0, \bar{S}=0$ then $\bar{S} \bar{R}$ latch will be a forbidden state as both $Q=1, \bar{Q}=1$.

### 3.7 Flip-Flop

The previous section dealt with latches which is a form of asynchronous sequential circuit. Any change in the input of the latch is immediately transmitted to the output. Such a situation is normally undesirable in digital electronics and further raise the need of a control signal which when triggered prompts the output to change. Therefore the operation of the latch can be modified by providing an additional control input which determines when the state of the circuit needs to be changed. This control input is termed as Clock or clock pulse. A latch with a clock pulse to control its operation works in a synchronous mode and is known as Flip-flop. The term synchronous indicates that the output changes its state only at specified point according to the input of the latch circuit.

There are many types of Flip-flops. The major difference lies in the number of inputs they process and the manner in which the inputs affect their output state. Various types of Flipflop are

- SR Flip-Flop
- D Flip-Flop
- JK Flip-Flop
- T Flip-Flop

In a sequential circuit the most basic and important memory element is Flip-flop which is made up of assembly of logic gates. A logic gate in itself incapable of storing any information but when wired together in a particular fashion can store information. A flip-flop can be defined as a binary storage device, capable of storing one bit of information.

### 3.7.1 S-R Flip-flop

As explained in the previous section, in a latch the output can change the state at any time as the input condition changes and in a Flip-flop an ENABLE (EN) input is chosen to control the state of the flip-flop. This ENABLE input can be clock. So a gated S-R Latch is also called as clocked S-R Latch/synchronous S-R Latch/S-R Flip-flop. In this case $S$ and $R$ input will control the state of flip-flop only when the ENABLE is HIGH. When the ENABLE is LOW, the input becomes ineffective and the output retains its previous state. The S-R latch with the ENABLE input is shown in the figure.

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Figure 7: Circuit diagram of S-R Flip-flop
From the figure 10 it can be depicted that the addition of two AND gates at the R and S inputs will result in a flip-flop that can be enabled or disabled. When the EABLE input is low then the output of both the AND gates will low so $S$ and $R$ input of the Latch will be at logic 0 . Table 3 gives the truth table for S-R flip-flop. From the truth table it can be verified that the output observes no change and retains its last value. When ENABLE is low the latch is said to be disabled and any change in the value of $S$ and $R$ input of the and gate results in no change at the output. When the ENABLE input is high the latch is said to be enabled and the input at $R$ and $S$ of the latch will follow the truth table given in table 1. The output will change in response to the input changes as long as the ENABLE is high.

| $\mathbf{R}$ | $\mathbf{S}$ | ENABLE (EN) | $\mathbf{Q}$ | Remarks |
| :---: | :---: | :---: | :---: | :---: |
| X | X | LOW | Last value | No change |
| 0 | 0 | HIGH | Last value | No change |
| 0 | 1 | HIGH | 1 | Set |
| 1 | 0 | HIGH | 0 | Reset |
| 1 | 1 | HIGH | $?$ | Forbidden |

Table 3: Truth table for gated S-R latch

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## Value addition

Determine the output waveform $Q$ if the inputs $S$ and $R$ as shown in the figure 8 are applied to gated S-R latch which is initially RESET.


Figure 8: Timing diagram

In a similar fashion a clock pulse is used to control the latch, in order to store the information at anytime and then hold the stored information for any desired period of time. This flip-flop is called a clocked R-S flip-flop. The clock signal is generally a rectangular pulse train or a square wave. The circuit diagram of clocked S-R flip-flop is shown in the figure 9.


Figure 9: Circuit diagram of clocked S-R flip-flop
Table 4 gives the truth table for clocked S-R flip-flop.

## Circuit Operation

Let us discuss the four cases as mentioned in the truth table (table 4):
When Clock=0
I. Let us assume $Q=0, \bar{Q}=1$

In this case, as clock is 0 so the output of N1 and N2 are both high. As $\bar{Q}=1$ and both the inputs of N3 NAND gate is at logic 1 so the output $\mathrm{Q}=0$. Similarly as 13
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$\mathrm{Q}=0$, the output of N4 NAND gate would be at logic 1 i.e. $\bar{Q}=1$. Therefore it is evident that the output doesn't change state when the clock is zero.
II. Let us assume $Q=1, \bar{Q}=0$

In this case, the output of the N1 and N2 NAND gates are high i.e. at logic 1. As $\bar{Q}=0$ and the output of N3 NAND gate will be at logic 1 so the output $\mathrm{Q}=1$. Similarly as $\mathrm{Q}=1$, both the input of N4 gate are at high level so the output of N4 NAND gate would be at logic 0 i.e. $\bar{Q}=0$. Therefore it is evident that the output doesn't change state when the clock is zero.

When the clock=1, the clock pulse is present, then the circuit operation is exactly same as that of S-R flip-flop of figure 7 .

| CLK | $\mathbf{R}$ | $\mathbf{S}$ | $\mathbf{Q}$ | $\bar{Q}$ | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | X | x | Last value | Last value | No change |
| 1 | 0 | 0 | Last value | Last value | No change |
| 1 | 0 | 1 | 1 | 0 | Set |
| 1 | 1 | 0 | 0 | 1 | Reset |
| 1 | 1 | 1 | $?$ | $?$ | Forbidden |

Table 4: Truth table for clocked S-R flip-flop.

### 3.7.2 D Flip-flop

The main problem with S-R Flip-flop is the forbidden state which occurs when both the inputs are at logic 1 . Such a condition may occur inadvertently and completely undesirable. Also in S-R flip-flop a high $S$ is required to SET the flip-flop and a high $R$ is required to RESET the flip-flop and thereby generation of two signals to drive a flip-flop is inconvenient in many applications. All such problems can prevail over by simply modifying the S-R flipflop. This very idea led to a new flip-flop which is known as D Flip-flop. D flip-flop requires a single data input and a clock input. D flip-flop is often called a delay flip-flop. The word delay describes what happens to the data or information at the input D. The data at the input $D$ is delayed one clock pulse from getting to output $Q$. The same can be verified from the truth table (table 5) where the output $Q$ follows input $D$ after one clock pulse $Q_{n+1}$.

| Clk | $\mathbf{D}$ | $\mathbf{Q}_{\mathbf{n + 1}}$ | Remarks |
| :---: | :---: | :---: | :---: |
| 0 | X | $\mathrm{Q}_{\mathbf{n}}$ | Last value |
| 1 | 0 | 0 | Reset |
| 1 | 1 | 1 | Set |

Table 5: Truth table of D flip-flop

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The logic symbol and the circuit diagram is given in figure


Figure 10: Logic symbol and circuit diagram of $D$ flip-flop.
When the clock is at logic 0 i.e. low, then both the AND gates are disabled and the input to both S and R inputs of $\mathrm{S}-\mathrm{R}$ flip-flop are at logic 0 level. Referring the truth table 3 for $\mathrm{S}-\mathrm{R}$ flip-flop it can be verified that the output remains the same and it retains the same state as the previous state. Thereby no change in the value of D would have any impact on the output, this condition is shown as a cross or a don't care condition in truth table. When the clock is high both AND gates are enabled and the data input at D is reflected at the output. This can be explained by taking two cases:

## Case 1:

When $\mathrm{Clk}=1$ and $\mathrm{D}=0$
Since the output of A1 AND gate is 0 and A2 AND gate is 1 , hence $S$ is at logic 0 and $R$ is at logic 1 level. When $S=0$ and $R=1$, it forces the flip-flop to reset. Thus when clk=1 and $D=0$, then $\mathrm{Q}_{\mathrm{n}+1}=0$ and resets the flip-flop.

## Case 2:

When $\mathrm{Clk}=1$ and $\mathrm{D}=1$
Since the output of A1 AND gate is 1 and A2 AND gate is 0 , hence $S$ is at logic 1 and $R$ is at logic 0 level. When $S=1$ and $R=0$, it forces the flip-flop to set. Thus when clk=1 and $D=1$, then $Q_{n+1}=1$ and sets the flip-flop.
When the clock again goes low the output retains the last value. Thus it can be emphasized that the output follows the data input as long as the clock pulse is at logic 1 level with just delay equal to propagation delay time for a gate, hence the name delay flip-flop.

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Try yourself
Draw D flip-flop using NAND gates only and explain its working.
Solution:


Figure 11: D flip-flop using NAND gates

## Circuit operation

1. When the clock pulse is at logic 0 level, then the output of N1 and N2 NAND gate is at logic 1 level (remember the thumb rule). Both the outputs retain their last value regardless of any value at $D$ input.
2. When the clock pulse is at logic 1 level

- When $D=0$, then output of N 1 gate is at 1 and that of N 2 is at 0 . Since one of the inputs of N4 is zero so the output of N4 is at 1. i.e. $\bar{Q}=1$. Since the output of N4 is connected to input of N3, so both the input of N3 NAND gate is at logic 1 , thereby forcing the output $\mathrm{Q}=0$.
When $\mathrm{Clk}=1$ and $\mathrm{D}=0$ then $\mathrm{Q}=0$ and it RESETs the flip-flop
- When $D=1$, then output of $N 2$ gate is at 1 and that of N1 is at 0 . Since one of the inputs of N3 is zero so the output of N3 is at 1. i.e. $\mathrm{Q}=1$ Since the output of N3 is connected to input of N4, so both the input of N4 NAND gate is at logic 0 , thereby forcing the output $\bar{Q}=0$. When $\mathrm{Clk}=1$ and $\mathrm{D}=1$ then $\mathrm{Q}=1$ and it SETs the flip-flop


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## Value Addition

Determine the Q output waveform if the input shown in the figure 12 is applied to gated D latch which is initially RESET.


Figure 12: Timing diagram

### 3.7.3 J-K Flip-flop

J-K flip-flop is a improved version of S-R flip-flop and is considered as "universal" flip-flop. It is a versatile and widely used flip-flop. If it is an improved version of S-R flip-flop then what could be the improvement. The improvement lies in the non-occurrence of forbidden state. The functioning of J-K flip-flop is identical to that of S-R flip-flop except to the last state where a J-K flip-flop "toggles". It is this unique feature which makes it useful in designing many digital circuits such as counters.

Toggle means to switch to the opposite binary state with each applied clock pulse

The logic symbol and the circuit diagram of J-K flip-flop is given in figure 13.


Figure 13: Logic symbol and the circuit diagram of J-K Flip-flop
Table 6 gives the truth table for J-K flip-flop.

| CLK | $\mathbf{J}$ | $\mathbf{K}$ | $\mathbf{Q}_{\mathbf{n + 1}}$ | Remarks |
| :--- | :--- | :--- | :--- | :--- |

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| 0 | X | X | $\mathrm{Q}_{\mathrm{n}}$ | No change |
| :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 0 | $\mathrm{Q}_{\mathrm{n}}$ | No change |
| 1 | 0 | 1 | 0 | Reset |
| 1 | 1 | 0 | 1 | Set |
| 1 | 1 | 1 | $\overline{Q_{n}}$ | Toggle |

Table 6: Truth table for J-K flip-flop

## Circuit operation

## Case 1:

When clock $=0$
Then both the AND gates A1 and A2 are disabled and then both the inputs have no effect on the output. The flip-flop will retain the last state and the output observes no change.

Case 2:
When $\mathrm{clk}=1, \mathrm{~J}=0$ \& $\mathrm{K}=0$
Again both the AND gates get disabled, leading the inputs $\mathrm{S}=\mathrm{R}=0$. Thus the output retains the last state and observes no change.

## Case 3:

When $\mathrm{clk}=1, \mathrm{~J}=0$ \& $\mathrm{K}=1$
The AND gate A1 is disabled and A2 is enabled. Since the output of A1 is zero so there is no chance to SET the flip-flop. The only possibility is to RESET it. When Q is high the output of A2 is high and passes a RESET trigger as soon as the next clock pulse arrives. So $\mathrm{Q}_{\mathrm{n}+1}=0$ i.e. the next clock pulse RESETs flip-flop (unless Q is already RESET).

## Case 4:

When $\mathrm{clk}=1, \mathrm{~J}=1 \& \mathrm{~K}=0$
Now the AND gate A2 is disabled and A1 is enabled. Since the output of A2 is zero so there is no chance to RESET the flip-flop. The only possibility is to SET it. When Q is low and $\bar{Q}$ is high then the output of A1 is high and passes a SET trigger as soon as the next clock pulse arrives. So $\mathrm{Q}_{\mathrm{n}+1}=1$ i.e. the next clock pulse SETs flip-flop (unless Q is already SET or high).

## Case 5:

When $\mathrm{clk}=1, \mathrm{~J}=1 \& \mathrm{~K}=1$

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This case makes the J-K flip-flop unique in comparison to S-R flip-flop. In S-R flip-flop if both the inputs are high then it is a forbidden state whereas in J-K flip-flop it is possible to SET or RESET the flip-flop. When both inputs are high then the output toggles. Toggle means to switch to the opposite binary state with each applied clock pulse. Let us understand the working of a J-K flip-flop with two examples:

- If $\mathrm{Q}=0 \& \overline{\mathrm{Q}}=1$

The output of AND gate $A 1=1$ and that of $A 2=0$. Since $S=1$ and $R=0$ so it will SET the flip-flop. The new output at the next clock pulse will be $\mathrm{Q}=1$ \& $\overline{\mathrm{Q}}=0$. Thus $\mathrm{Q}_{\mathrm{n}+1}=\overline{Q_{n}}$ and the output toggle on the next clock pulse.

- If $\mathrm{Q}=1 \& \overline{\mathrm{Q}}=0$

The output of AND gate $A 2=1$ and that of $A 1=0$. Since $S=0$ and $R=1$ so it will RESET the flip-flop. The new output at the next clock pulse will be $\mathrm{Q}=0$ \& $\overline{\mathrm{Q}}=1$. Thus $\mathrm{Q}_{\mathrm{n}+1}=\overline{Q_{n}}$ and the output toggle on the next clock pulse.

## Try yourself

Draw J-K flip-flop using NAND gates only and explain its working (figure 14).
Solution:


Figure 14: J-K flip-flop using NAND gates only
Circuit operation
Let us assume that clock is high for all the cases
Case 1:
$\mathrm{J}=0, \mathrm{~K}=0$, initially $\mathrm{Q}=0 \& \overline{\mathrm{Q}}=1$
As $\mathrm{J}=\mathrm{K}=0$ so the output of both NAND gates N 1 and N 2 is at logic 1 . As $\mathrm{Q}=0$ so the output of N4 is 1 and hence the input of N3 are both at logic 1, forcing it to give a low output. Therefore it can be verified that $\mathrm{Q}=0 \quad \mathrm{Q}=1$ and the flip-flop retains its last value and observes no change in the output. The same can be verified when $\mathrm{Q}=1$ \& $\overline{\mathrm{Q}}=0$.
Students are encouraged to verify all the remaining cases on their own.

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## Do you know?

According to P. L. Lindley, a JPL engineer, the flip-flop types (RS, D, T, JK) were first discussed in a 1954 UCLA course on computer design by Montgomery Phister, and then appeared in his book Logical Design of Digital Computers. Lindley was at the time working at Hughes Aircraft under Eldred Nelson, who had coined the term JK for a flipflop which changed states when both inputs were on (a logical "one"). The other names were coined by Phister. Lindley explains that he heard the story of the JK flip-flop from Eldred Nelson, who is responsible for coining the term while working at Hughes Aircraft. Flip-flops in use at Hughes at the time were all of the type that came to be known as J-K. In designing a logical system, Nelson assigned letters to flip-flop inputs as follows: \#1: A \& B, \#2: C \& D, \#3: E \& F, \#4: G \& H, \#5: J \& K. Nelson used the notations "j-input" and " $k$-input" in a patent application filed in 1953.

Source : http://en.wikipedia.org/wiki/Flip-flop_(electronics)

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### 3.8 Summary

- In sequential circuits, the output at any instant of time depends on the present value of the input as well as on the past outputs also.
- Sequential circuits are classified as Asynchronous and synchronous, depending on the timing of the signal.
- Latches are bistable devices whose state normally depends on asynchronous inputs.
- A latch with a clock pulse to control its operation works in a synchronous mode is known as flip-flop.
- Symbols and truth table for latch and flip-flops are summarized below:

| Latch/ Flip-flop | Logic Symbol | Truth Table |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| S-R <br> Latch (active high) |  | R | S | Q |  | arks |
|  |  | 0 | 0 | Las valu |  | ange |
|  |  | 0 | 1 | 1 | - | St |
|  |  | 1 | 0 | 0 |  | set |
|  |  | 1 | 1 | ? | Forb | idden |
| S-R <br> Latch (active low) | $f^{\bar{S}} \begin{array}{cc} \bar{R} & \bar{Q} \end{array}$ | $\bar{R}$ $\bar{S}$ $\mathbf{Q}$ Remarks <br> 0 0 $?$ Forbidden <br> 0 1 0 Reset <br> 1 0 1 Set <br> 1 1 $\begin{array}{c}\text { Last } \\ \text { value }\end{array}$ $\begin{array}{c}\text { No } \\ \text { change }\end{array}$ |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
| Clocked S-R Flipflop |  | CLK | R | S | Q | Remarks |
|  |  | 0 | X | X | Last <br> value | No change |
|  |  | 1 | 0 | 0 | Last value | No change |
|  |  | 1 | 0 | 1 | 1 | Set |
|  |  | 1 | 1 | 0 | 0 | Reset |
|  |  | 1 | 1 | 1 | ? | Forbidden |

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Institute of Lifelong Learning, University of Delhi

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- Waveform (timing) diagrams are used to describe the operation of sequential circuits.


### 3.9 Exercise

### 3.9.1 Subjective Questions

1. Differentiate between combinational circuits and sequential circuits.
2. What is the fundamental difference between a latch and a flip-flop.
3. Distinguish between synchronous and asynchronous latch.
4. Why D flip-flop is called as transparent flip-flop.
5. Give the advantage of a J-K flip-flop over S-R flip-flop.
6. Draw the output waveform of active high $S-R$ flip-flop when the given input waveforms are applied.

7. If the waveform are applied to active low S-R latch assume the latch to be initially SET, draw the output waveform.

8. If $D$ input of $D$ flip-flop changes from low to high in the middle of the positive going clock edge

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(1) Describe what happens if the flip-flop is positive edge triggered
(2) Describe what happens if the flip-flop is a Master-Slave flip-flop.

### 3.9.2 Multiple Choice Questions

1) When $R=1$ and $S=1$ in $S$ - $R$ flip-flop then

| A) $Q=0$ | B) $Q=1$ |
| :--- | :--- |
| C) $Q$ will toggle | D) Forbidden state |

2) If both synchronous and asynchronous inputs on a J-K flip-flop are activated which input will control the output

| A) Clock input | B) Synchronous input |
| :--- | :--- |
| C) Asynchronous input | D) both $a$ and b |

3) A feature that distinguishes $\mathrm{J}-\mathrm{K}$ flip-flop from S-R flip-flop

| A) number of inputs | B) number of outputs |
| :--- | :--- |
| C) type of clock | D) Toggling condition |

4) Flip-flop is an example of which multivibrator

| A) Astable | B) Monostable |
| :--- | :--- |
| C) Bistable | D) None of the above |

5) When $\mathrm{J}=1$ and $\mathrm{K}=0$ the output of the flip-flop is

| A) RESET | B) SET |
| :--- | :--- |
| C) Forbidden state | D) will retain last value |

6) Which of the following is the simplest memory element
A) Flip-flop
B) Logic gate

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| C) control line | D) Inverter |
| :--- | :--- |

7) The forbidden state of S-R flip-flop is when

| A) $S=1, R=0$ | B) $S=0, R=1$ |
| :--- | :--- |
| C) $S=0, R=0$ | D) $S=1, R=1$ |

8) Which of the following is not a flip-flop

| A) D | B) T |
| :--- | :--- |
| C) Z | D) All of the above |

Answers to Multiple Choice Questions:

1) Forbidden state

Justification: When both the inputs of S-R flip-flop is high then it is an illegal state hence forbidden.
2) Asynchronous input

Justification: Asynchronous inputs such as PRESET will set the flip-flop and forces the output $\mathrm{Q}=1$ and a high CLEAR will reset the flip-flop which forces the output $\mathrm{Q}=0$ irrespective of the clock input or even the data input.
3) Toggling condition

Justification: When both the inputs in J-K flip-flop are high then it result in togeling condition whereas in S-R flip-flop it is a forbidden state.
4) Bistable

Justification: In a bistable state both states are stable and in a flip-flop both states are stable states.
5) SET

Justification: When J=1 and $=0$ it SETs the flip-flop.
6) Flip-flop

Justification: Flip-flop is the simplest memory element,
7) $\mathrm{S}=1, \mathrm{R}=1$

Justification: When $\mathrm{S}=1$ and $\mathrm{R}=1$, it leads to forbidden state in a S-R flip-flop.
8) $Z$

Justification: Z flip-flop doesn't exist and D or T are types of flip-flop.

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### 3.10 Glossary

Bistable Having two stable states. Flip-flops and latches are bistable multivibrators.
Clock The basic timing signal in a digital system; a periodic waveform in which the interval between pulses equals the time for one bit.

D Flip-flop A type of bistable multvibrator in which the output assumes the state of the D input on the triggering edge of the clock pulse.

Flip-flop A basic storage circuit that can store only one bit at a time; a synchronous bistable device.

J-K flip-flop a type of flip-flop that can operate in the SET-RESET, no change and toggle mode.

Latch A bistable digital circuit used for storing a bit.
Multivibrator A class of digital circuits in which the output is connected back to the input to produce either two stable states, one stable states or no stable states depending on the configuration.

S-R flip-flop a SET-RESET flip-flop that can operate in the SET-RESET, no change and forbidden state.

Timing diagram A graph of digital waveforms showing the proper time relationship of all the waveforms and how each waveform changes in relation to the others.

Toggle the action of a flip-flop when it changes state on each clock pulse.

### 3.11 Reference Books:

* Digital Principles \& Applications, A.P.Malvino, D.P.Leach \& Saha, 7th Ed., 2011, Tata McGraw
* Fundamentals of Digital Circuits, A. Anand Kumar, 2nd Edition, 2009, PHI Learning Pvt. Ltd.
* Digital Electronics, Principles and applications, Roger L Tokheim, 2003, Tata McGraw Hill.
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* Digital Electronics, An introduction to theory and practice, W H Gothmann, 1982, PHI Learning.

