Logic Gates

Basic logic circuits with one or more inputs and one outputs are known as gates. Gates are used as the building blocks in the design of more complex digital logic circuits. We will now describe commonly used gate

AND Gate

The output of and gate is high (1) if and only if all its inputs are high (1) If any one or more of its inputs are low (0), the output of the gate is low (0). This is referred to as a coincidence gate.

Boolean Expression $Y = A \cdot B$

Truth Table. For two variables ($n = 2$)

	A	B	A·B = Y
1	0	0	0
2	0	1	0
3	1	0	0
4	1	1	1

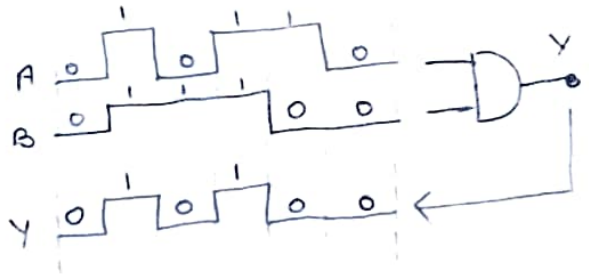
$2^n = N$

N – total number of possible combinations.

for $n = 2$, $N = 2^2 = 4$, combinations

$n = 3$, $N = 2^3 = 8$, combinations

Pulsed Operation



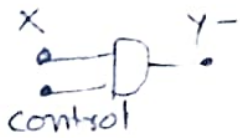
Application: AND gate as an enable/Inhibit device.

A common application of AND gate is to enable (to allow) the passage of a signal (pulse wave form) from one point to another point at certain time and to inhibit (prevent) the passage at others time.

To use AND gate as Inhibit / Enable device one of its input terminal is used as control / Enable terminal. where, as, information is applied at the other input terminal. The truth for AND gate as Inhibit / Enable device is as under

control or Enable.	Data. X	output Y	
0	X	0	Inhibit
0	X	0	
1	X	X	Enabled
1	X	X	

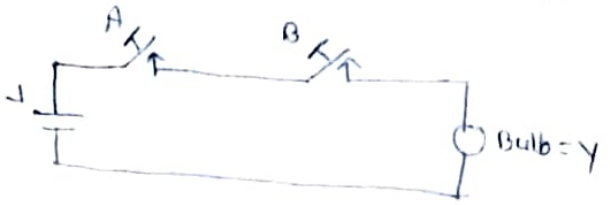
Here X may be 0
X may be 1



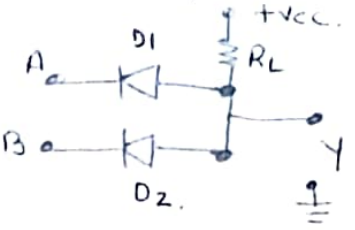
From this truth table we can say that when control is 0, output is 0 and in independent of X (Input value). So and gate is not functioning. or AND gate is Inhibited. It means that it is not passing the data/input.

when control is 1. then $Y = X$, ie if $X = 0$, $Y = 0$. or if $X = 1$, then $Y = 1$. It means that output value is equal to input value. or we can say that Input is passed through the gate. or AND gate is enabled.

(a). Electrical Equivalent Circuit



(b). using diode logic.



Close = 1, open = 0, Bulb glow = 1
Bulb off = 0

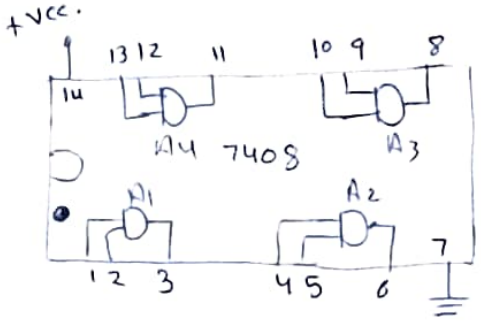
A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

(i) when A=0 & B=0. Both diodes are Forward biased so Y = 0.6 or Y = 0

(ii) when A=0, D1 is forward biased and B = 1, D2 is reversed biased so Y = 0.6 Y = 0

(iii) when B=0, D2 is forward biased and A=1, D1 is reverse biased. so Y = 0.6 Y = 0

(iv) when both A = B = 1, both diodes are reverse biased so Vo = +Vcc = 1. (0 = 0 Level)



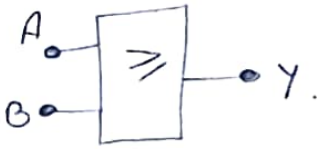
2 input Quad AND gate.

Input pins :- Gate A1 - 1, 2 ——— output pin 3
A2 - 4, 5 ——— 6
A3 = 9, 10 ——— 8
A4 = 12, 13. ——— 11

OR-GATE

The output of OR-gate is high (1) if any or all the inputs are high (1). When all the inputs are Low (0), the output of the gate is Low (0).

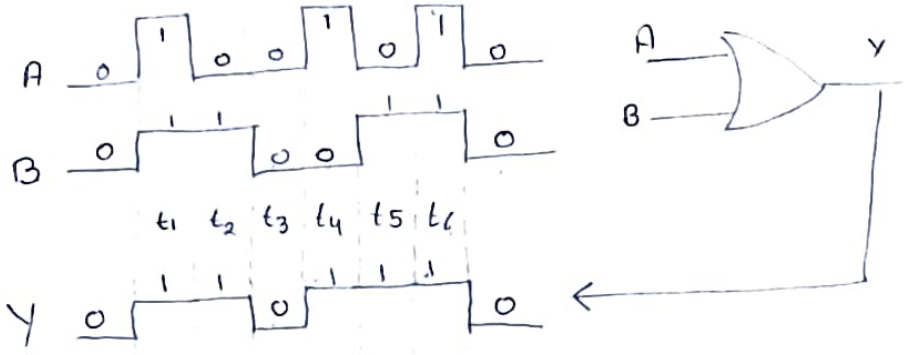
$Y = A + B$



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Pulsed operation:



During time intervals

t_1, A = 1, B = 1, Y = 1

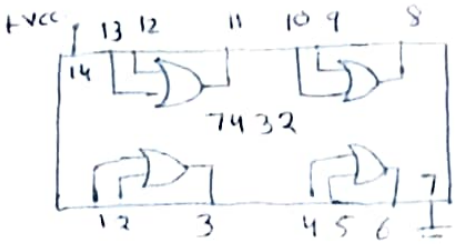
t_2, A = 0, B = 1, Y = 1

t_3, A = 0, B = 0, Y = 0

t_4, A = 1, B = 0, Y = 1

t_5, A = 0, B = 1, Y = 1

t_6 A = 1, B = 1, Y = 1



2 input quad OR gate-IC.

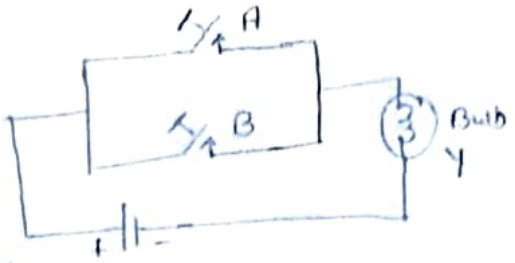
Input pins: 1, 2, 4, 5, 9, 10 & 12, 13.

output pins: 3, 6, 8 and 11,

pin 7 : GND

pin 14 : +Vcc.

Electrical Equivalent



open = 0
close = 1
Bulb Glow = 1
Bulb off = 0

Switches

If A = 1, close, B open, Bulb glow (1)

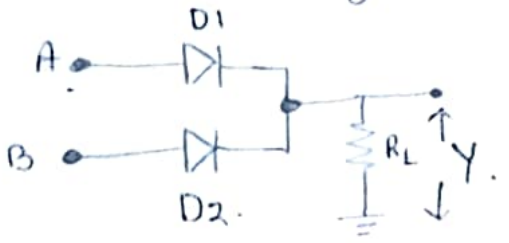
B = close (1) A = open (0), Bulb glow (1).

B = close (1), A = close (1), Bulb glow (1)

B = 0 (open), A = open (0), Bulb off (0)

A	B	Y = A+B
1	0	1
0	1	1
1	1	1
0	0	0

OR- Gate using Discrete Component - Diode Logic.



A	B	Y = A+B
0	0	0
1	0	1
0	1	1
1	1	1

working.

(i) A=0, B=0, Diodes D_1 and D_2 are reverse biased, (and will not conduct, so Y=0.

(ii) A = 1, Diode D_1 forward biased — conduct
B = 0 Diode D_2, Reverse biased — OFF,
Y = 1.

(iii) A = 0, Diode D_1, Reverse biased — OFF
B = 1 Diode D_2, Forward biased — ON, conduct.
So. Y = 1.

(IV) A = 1, Diode D_1, Forward biased — ON/ conduct.
B = 1, Diode D_2, Forward biased — ON/ conduct.
Y = A.

How to Inhibit/ Enable OR gate:

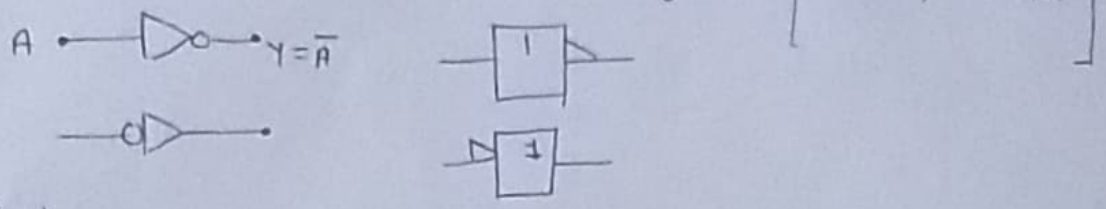
C Control	Data	output Y = C + X	
0	X = 0 =	0 = X	Enabled
0	X = 1	1 = X	
1	0	1	Inhibit
1	1	1	

OR gate is enabled when control/Enable/Inhibit input is '0'. Input passes through gate. output is equal to input. It is Inhibited when control/Enable/Inhibit Input is '1' and in inhibited state its output is High (1).

NOT Gate : Inverter

The inverter performs the operation called inversion or complementation.

Logic symbols are shown in figure. [ANSI / IEEE.]



Boolean expression $Y = \bar{A}$.

Truth table.

A	Y
0	1
1	0

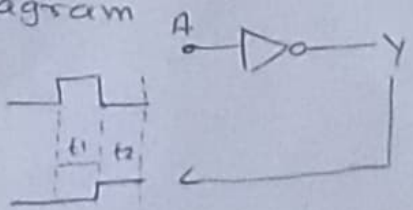
Here '0' (bubble) indicates inversion. It can appears on the input or output of any logic element, as shown above in fig.

(i) When appearing on the input, the bubble means that 0 is active input state, an the input is called active low input.

(ii) When appearing on the output, the bubble means that 0 is active or asserted output state, and output is called active low output.

(iii) The absence of bubble on input and output means that 1 is the active or asserted, and in this case the input or output ~~means that~~ is called active high.

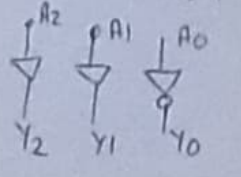
Timing Diagram



t_1 – A = 1, Y = 0

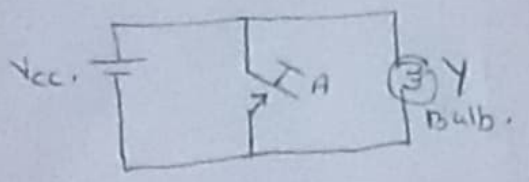
t_2 – A = 0, Y = 1

Application Not gate is used for producing 1's complement of a number.



A_2 A_1 A_0
1 0 1
Y_2 Y_1 Y_0
0 1 0

Electrical equivalent



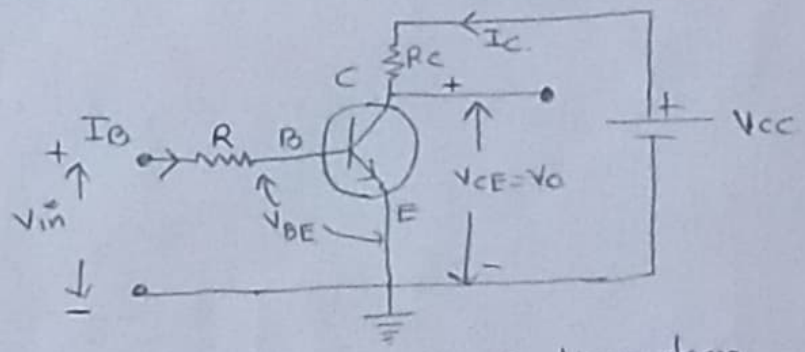
switch close = 1 ,
open = 0

Bulb glows = 1
bulb not glows = 0

when switch close, circuit gets short circuited, so no current flows through the bulb, so bulb off.
when switch is open, all current passes through bulb and it glows (1).

A	Y
0	1
1	0

: Not gate using Transistors:



NPN transistor in C-E configuration.

$$\beta = \frac{I_c}{I_B} \quad \text{— (1)}$$

For output loop $I_c R_c + V_{CE} - V_{cc} = 0$

$$V_{CE} = V_o = V_{cc} - I_c R_c \quad \text{— (2)}$$

For Input loop $I_B R + V_{BE} - V_{in} = 0$

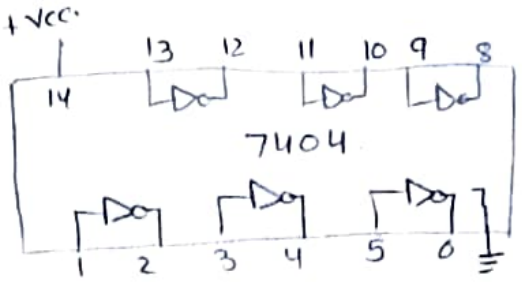
$$I_B = \frac{V_{in} - V_{BE}}{R} \quad \text{— (3)} \qquad V_{BE} = 0.7\ V$$

working $V_{in} = A = 0$. $I_B = 0$ [Because Emitter base junction is reversed bias so $I_c = 0$. ie Transistor is off.

From (2) $V_o = V_{cc}$ [High = 1]

$V_{in} = A$ = High, I_B is high [Emitter base junction F. Biased]
I_c will be high. [from 1, since β is constant and high]
ie Transistor is ON, $I_c R_c \approx V_{cc}$.

$V_o = 0$. (LOW).



Input pins :- 1, 3, 5, 9, 11, 13.

Output pins :- 2, 4, 6, 8, 10, 12.

GND = 7 pin

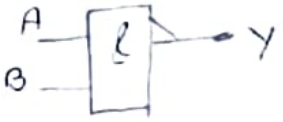
+Vcc = 14 pin.

NAND GATE

NAND gate is a circuit that produces Low (0) on its output only when all of its inputs are High (1). If any of the input is low, then output is high.

This gate is combination of AND and NOT gate.

Symbol



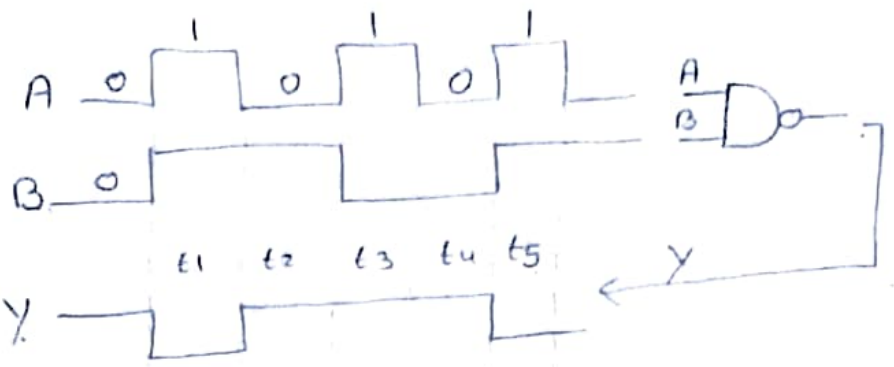
Boolean Expression

$$Y = \overline{A \cdot B}$$

Truth table:

A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

Wave form operation



During time intervals:-

t_1, $A=1$, $B=1$, $Y = \overline{A \cdot B} = \overline{1} = 0$

t_2, $A=0$, $B=1$, $Y = \overline{A \cdot B} = \overline{0} = 1$

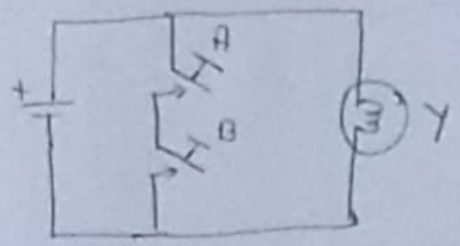
t_3, $A=1$, $B=0$, $Y = \overline{A \cdot B} = \overline{0} = 1$

t_4, $A=0$, $B=0$, $Y = \overline{A \cdot B} = \overline{0} = 1$

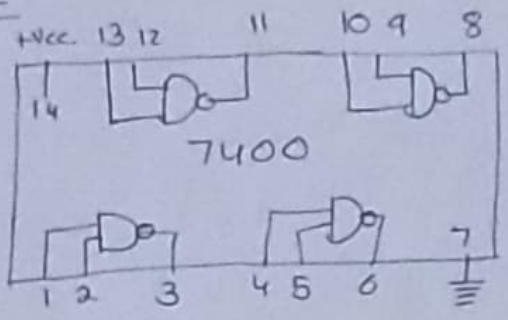
t_5, $A=1$, $B=1$, $Y = \overline{A \cdot B} = \overline{1 \cdot 1} = \overline{1} = 0$

D.T.L NAND gate [using diode transistor logic].

Electrical Equivalent



NAND Gate IC



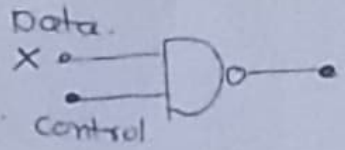
Input pins:- 1, 2, 4, 5
9, 10, 12, 13.

output pins:- 3, 6, 8, 11.

7 → GND

14 → +Vcc.

Inhibit / Enable NAND Gate:



Here X may be 0 or 1

$1 \cdot X = X$

Inputs.		outputs
control C	Data	$Y = \overline{C}X$
0	X	1
0	X	1
1	X	$\overline{X}$
1	X	$\overline{X}$

output locked at 1

(i) when control = 0, output is locked at 1. So gate is inhibit.

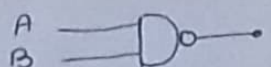
(ii) when control is High (1). output will be complemented

if $X = 0$, $Y = 1$

$X = 1$ $Y = 0$.

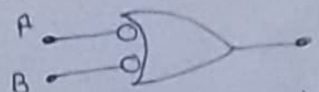
So we can say that data passes through the gate after inversion.

Equivalent of NAND gate



Truth table

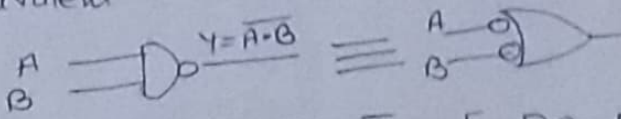
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



Truth table for bubbled OR-gate.

A	$\overline{A}$	B	$\overline{B}$	$\overline{A}+\overline{B}=Y$
0	1	0	1	1
1	0	0	1	1
0	1	1	0	1
1	0	1	0	0

Truth table of NAND gate is same as that of bubbled OR-gate. So we can say Bubbled OR gate is equivalent to NAND gate

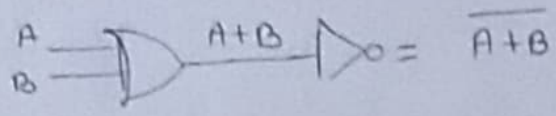


$$\overline{A\cdot B} = \overline{A}+\overline{B} \quad [\text{De-Morgan's Theorem}]$$

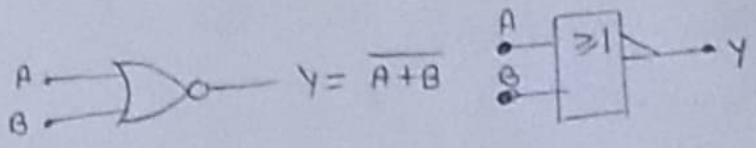
We can also say NAND gate performs a negative OR gate operation.

NOR- Gate

NOR operation = OR + NOT



Logical sysbd

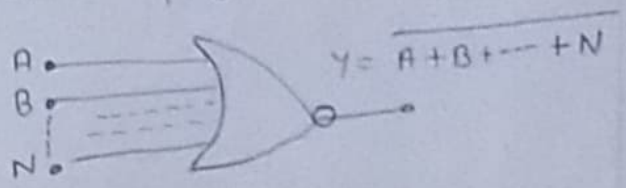


Statement: A NOR gate produces a Low output when any of its inputs is High. It produces High output when all of its inputs are Low.

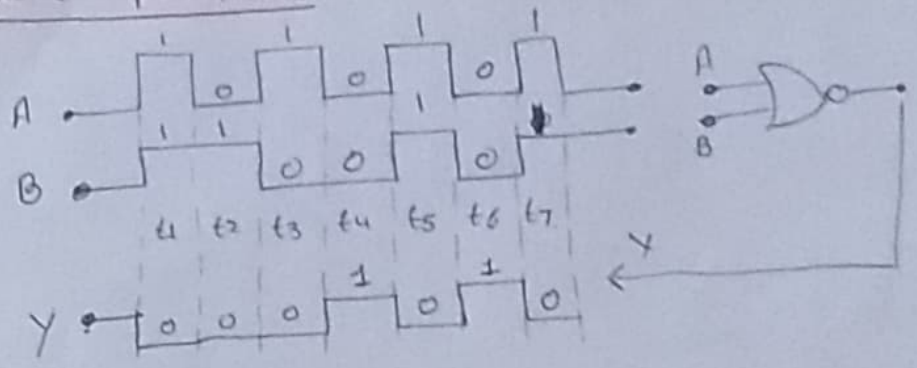
Truth table:

A	B	Y= $\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

For N inputs



Pulsed operation



During time intervals

t_1, t_5, t_7: A=1, B=1 $Y = \overline{A+B}$, $\overline{1+1} = 0$

t_2: A=0, B=1 $Y = \overline{A+B}$, $\overline{0+1} = \overline{1} = 0$

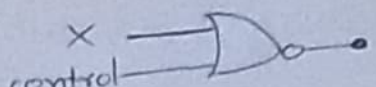
t_3: A=1, B=0 $Y = \overline{A+B}$, $\overline{1+0} = \overline{1} = 0$

t_4, t_6: A=0, B=0 $Y = \overline{A+B}$ $\overline{0+0} = \overline{0} = 1$

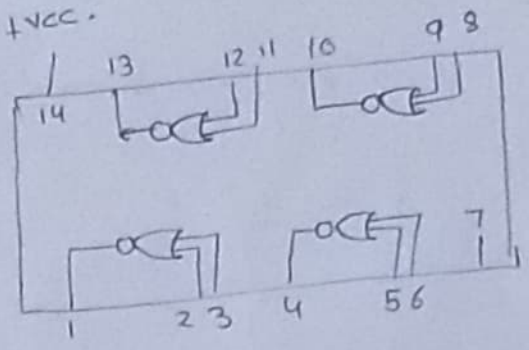
~~t_5: A=1, B~~

NOR gate Inhibit / Enable.

X date. It may be 0 or 1.



Inputs		output	Result
control	Data X	Y	
0	X	$\overline{0+X} = \overline{X}$	Data passes through gate after inversion.
0	X		
1	X	$\overline{1}$	output locked at Zero
1	X		
	1+X =	1	compare X and Y. $Y = \overline{X}$
0	1	0	complement of Data
0	0	1	
1	0	0	~~Data~~ output is locked at $\overline{0}$
1	1	0	



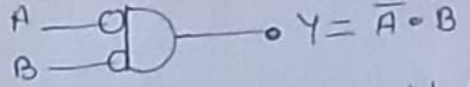
Input pins: 2, 3, 5, 6, 8, 9, 11, 12.

output pins: 1, 4, 10, 13.

7 pin – GND

14 pin – +Vcc.

Negative AND gate equivalent of NOR gate.



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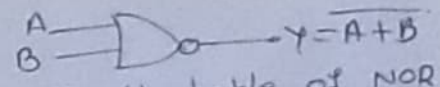

Truth table of Bubbled AND gate.

A	B	$\overline{A}$	$\overline{B}$	$Y = \overline{A} \cdot \overline{B}$
0	0	1	1	1
1	0	0	1	0
0	1	1	0	0
1	1	0	0	0

Truth table of NOR gate.

A	B	Y
0	0	1
1	0	0
0	1	0
1	1	0

Truth tables of Bubbled AND gate / negative AND gate is same as that of NOR gate.

$\overline{A+B} = \overline{A} \cdot \overline{B}$ DeMorgan Theorem

complemend of sum is equal to the product of complements.

Equivalend of NOR gate is bubbled AND gate.