~~Arithmet~~

Arithmetic circuits:

(i) Half Adder, (ii) Full adder (iii) Half subtractor and (iv) Full subtractor. (v). 4 bit binary Adder/ subtractor.

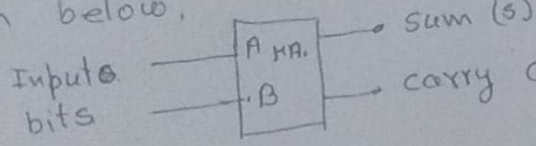
Rules of Binary addition are shown in table below

Augend col I (A)	Addend col II (B)	Sum col III (S)	Carry col IV (C)	Result
0	0	0	0	0
0	1	1	0	1
1	0	1	0	1
1	1	0	1	10

Table-I

Half-Adder:

The combinational logic circuit that perform addition operation on two bits is called Half adder circuit and the circuit that is capable of adding 3 bits is called full-adder. A Half-Adder adds two bits and produces a sum and a carry output. Logic symbol for a half-adder is shown below.



The first three column of table I, represents truth table of EX-OR gate, and first, second and IV column represent truth table of AND gate.

~~Carry is repr~~

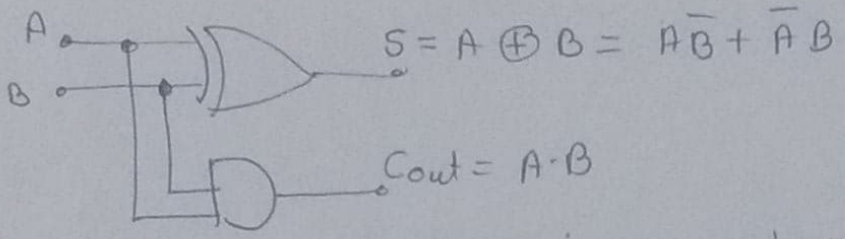
The sum can therefore be expressed as the exclusive-OR gate of the input variable.

$$S = \Sigma = A \oplus B \quad \text{—} \quad (1)$$

Carry Cout can be expressed as the AND gate of the input variables.

$$Cout = A \cdot B. \quad \text{—} \quad (2)$$

From equations (1) and (2), the logic implementation required for the half-adder function can be developed. The output carry is produced with an AND gate with A & B on the inputs, and the sum output is generated with an exclusive-OR gate as shown in fig. below.



Truth table for Half-Adder is as under:

A	B	S	Cout
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1
		X-OR	AND gate

Design half-adder using basic gates.

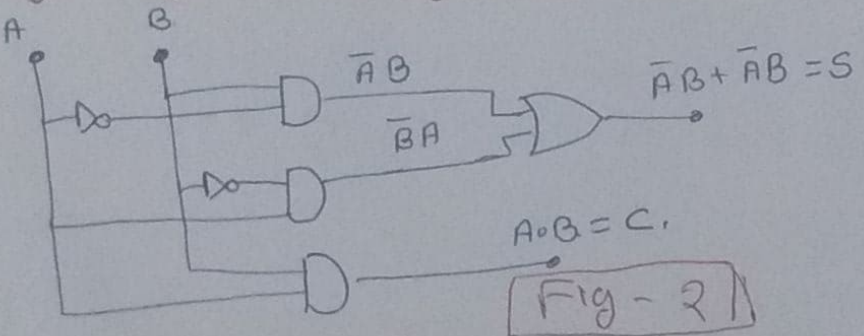
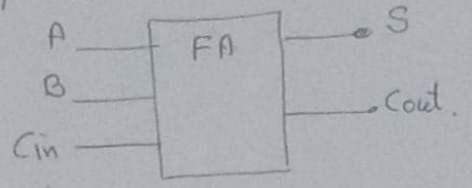


Fig - 2

Full-Adder

Full-adder is a combinational logic circuit that adds two bits and a carry coming from the lower order bits and outputs a sum and a Carry bit.

Logical Symbol.



No of rows = $2^n = 2^3 = 8$.

Truth Table.

Cin	A	B	S	Cout	
0	0	0	0	0	m_0
0	0	1	1	0	m_1
0	1	0	1	0	m_2
0	1	1	0	1	m_3
1	0	0	1	0	m_4
1	0	1	0	1	m_5
1	1	0	0	1	m_6
1	1	1	1	1	m_7.
Inputs			outputs.		

Full-adder using two Half-adder.

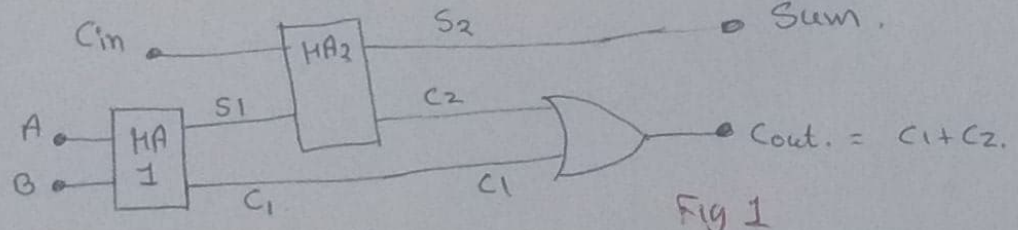


Fig 1

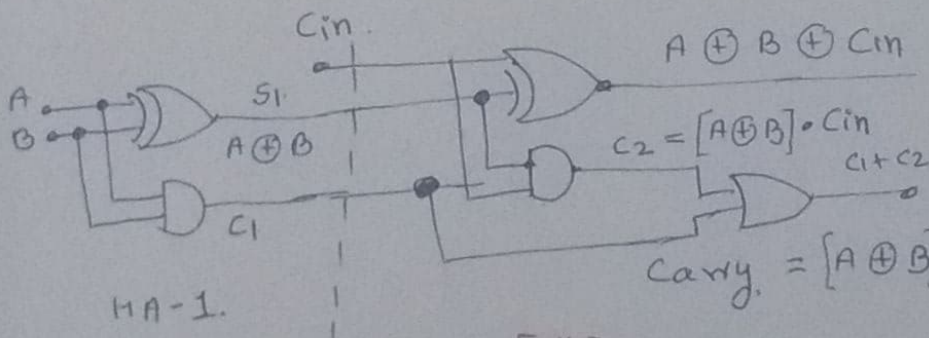


Fig 2

Simplify the logic circuit using K-Map [Minimised circuit]

Sum.

	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
$\bar{C}_{n-1}$	0	(1) 2	6	(1) 4
C_{n-1}	(1) 1	3	(1) 7	5

$Y = \Sigma(2,4,1,7)$.

$Y = \bar{A}\bar{B}C_{n-1} + \bar{A}B\bar{C}_{n-1} + ABC_{n-1} + A\bar{B}\bar{C}_{n-1}$

Carry.

	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
$\bar{C}_{n-1}$	0	2	(1) 6	4
C_{n-1}	1	(1) 3	(1) 7	(1) 5

$Y = \Sigma(3,5,6,7)$.

$Y = \bar{A}BC_{n-1} + A\bar{B}C_{n-1} + AB\bar{C}_{n-1} + ABC_{n-1}$

$Y = BC_{n-1} + C_{n-1}A + A \cdot B$ [Minimised].

See fig. (4)

~~and fig 3~~

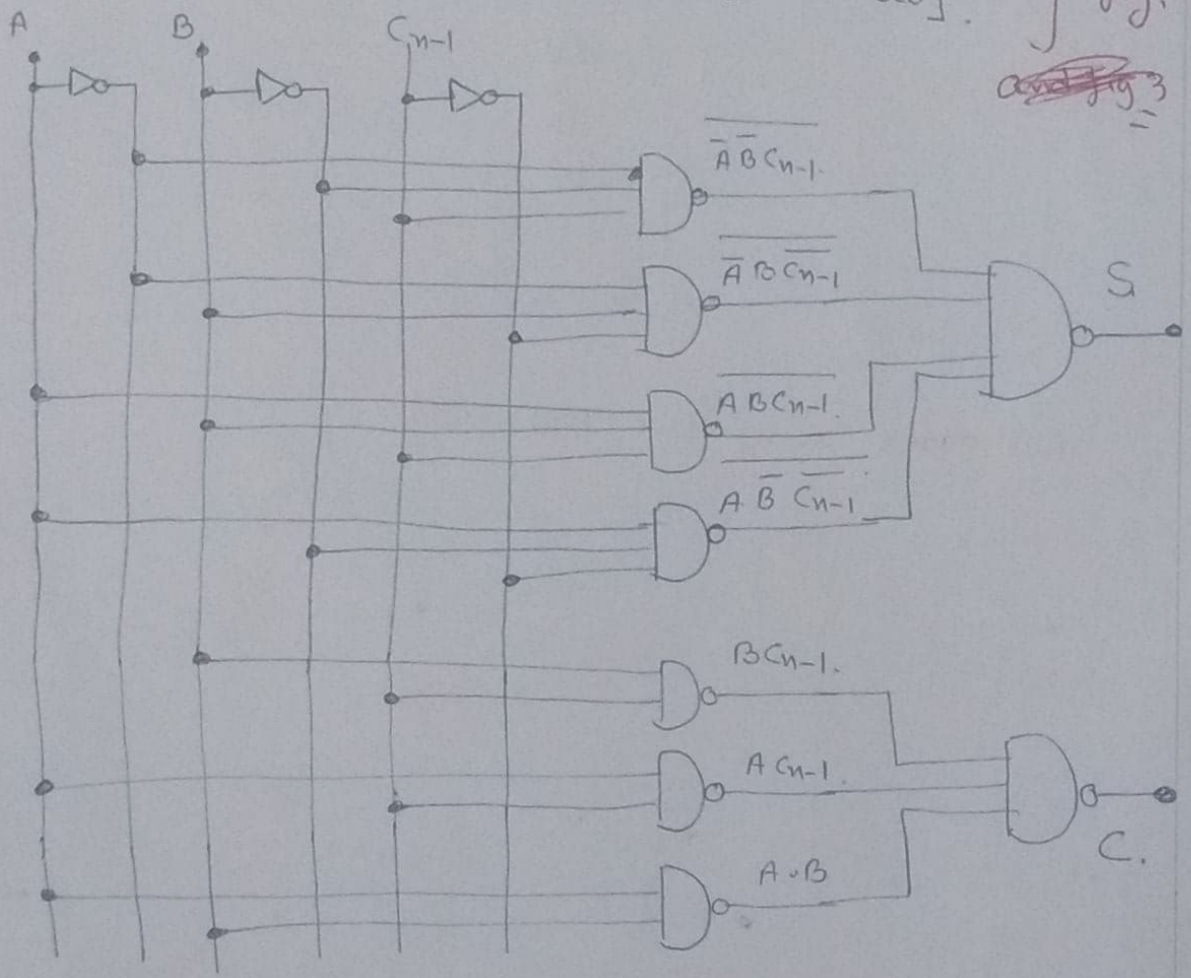
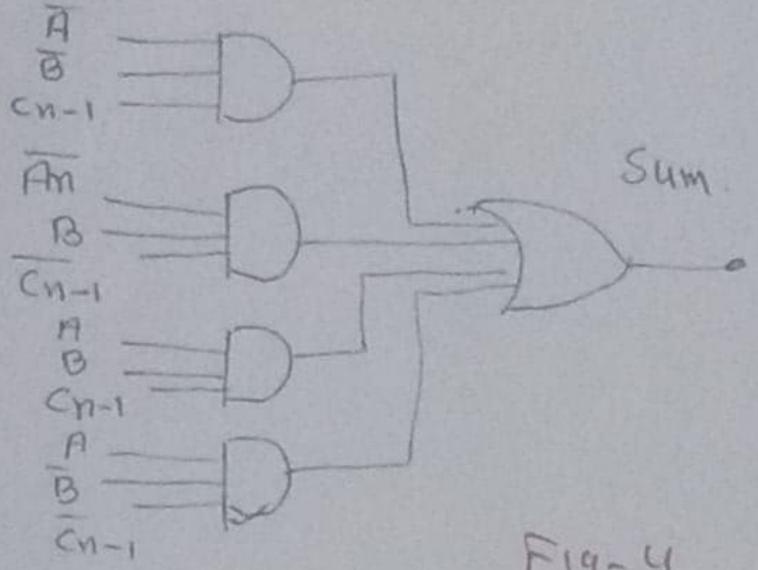


Fig. 3

Full Adder using A.O NOT gate. Minimised circuit

Sum



Carry

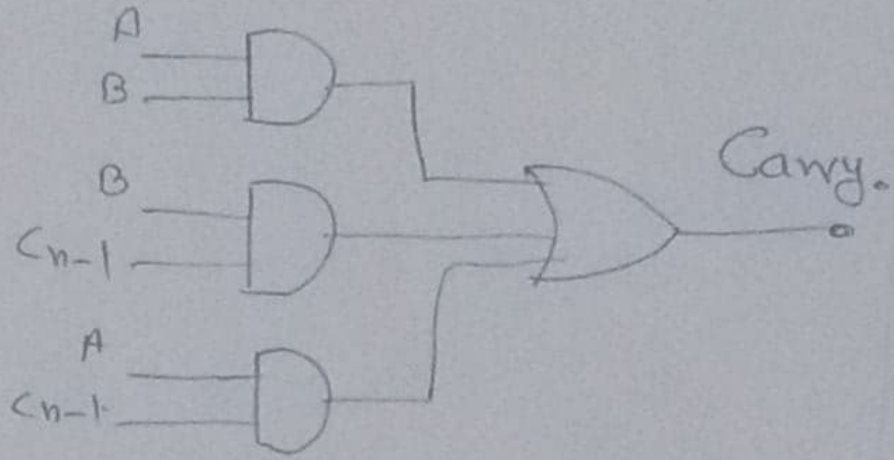


Fig-4

Full adder can also be realised using universal