Multiplexer

Multiplexing means sharing:

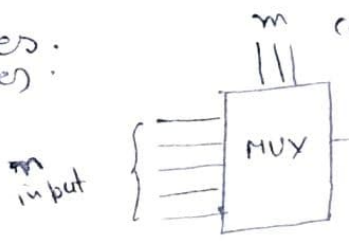
- Time
- Frequency.

A common example of multiplexing occurs when several peripheral devices share a single transmission line or bus to communicate with a computer. For this each device in succession is allocated a brief time to send or receive data. At a given time, one and only one device is ~~being~~ using the line. This is an example of time multiplexing.

In frequency multiplexing, several devices share a common line by transmitting at different frequencies

Multiplexer (MUX) or data selector is a combinational logic circuit that accepts several data inputs (m) and allows only one of them at a time to get through to output. The routing of desired data input to the output is controlled by 'n' controll lines.

logical symbol

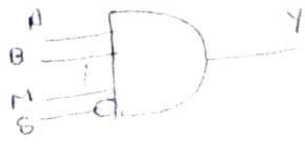


$n = 2^m$

n	m
16	4
8	3
4	2
2	1

16:1 MUX
8:1
4:1
2:1 multiplexer.

Inhibit operation



$Y = A \cdot B \cdot C \cdots M \cdot \overline{S}$

S	A	B	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1

S=	Y
1	0
1	0
A	0
B	0

It is called active low

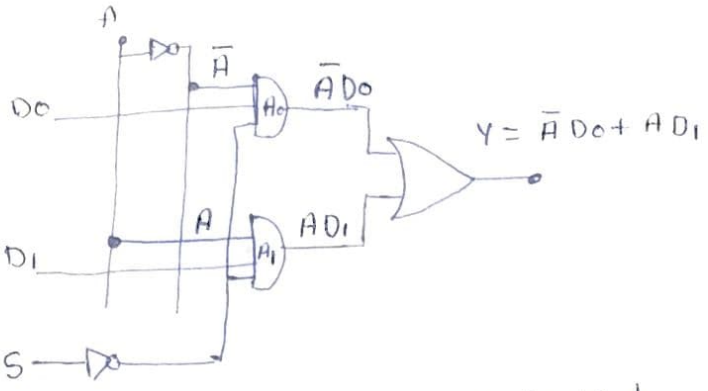
For S=0, And gate becomes enabled, so circuit.

If A ... M=1, S=0, then Y=1, so coincidence of A to M is allowed (coincidence circuit)

If A ... M=1, S=1, Y=0, Disabled operation, or Inhibit so coincidence is inhibited.

Example: 2:1 multiplexer.

$n = 2, \quad n = (2)^m \quad m = 1.$



A	Y
0	D_0
1	D_1

Working: $S = 1$, MUX is disabled

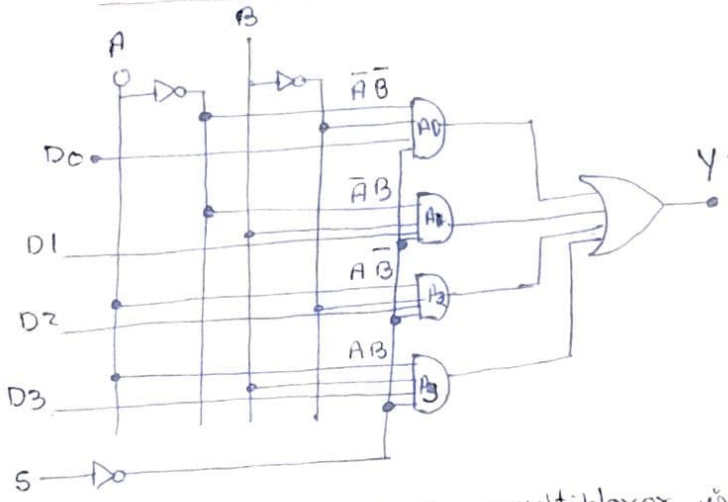
$S = 0$, Multiplexer is enabled.

$A = 0$, A_0 gate is enabled and and gate A_1 is disabled so $Y = \bar{A}D_0$

$Y = D_0$

$A = 1$, AND gate A_0 is disabled and AND gate A_1 is enabled so $Y = D_1$

4:1 Multiplexer



Working when $S = 1$, multiplexer is disabled.

$S = 0$ Multiplexer is enabled.

S	A	B	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	x	x	0

$A = 0, B = 0$

AND gate A_0 enabled, A_1, A_2, A_3 Disabled

$Y = D_0$.

$A = 0, B = 1$ and

AND gate A_1 enabled, A_0, A_2, A_3 disabled

$Y = D_1$

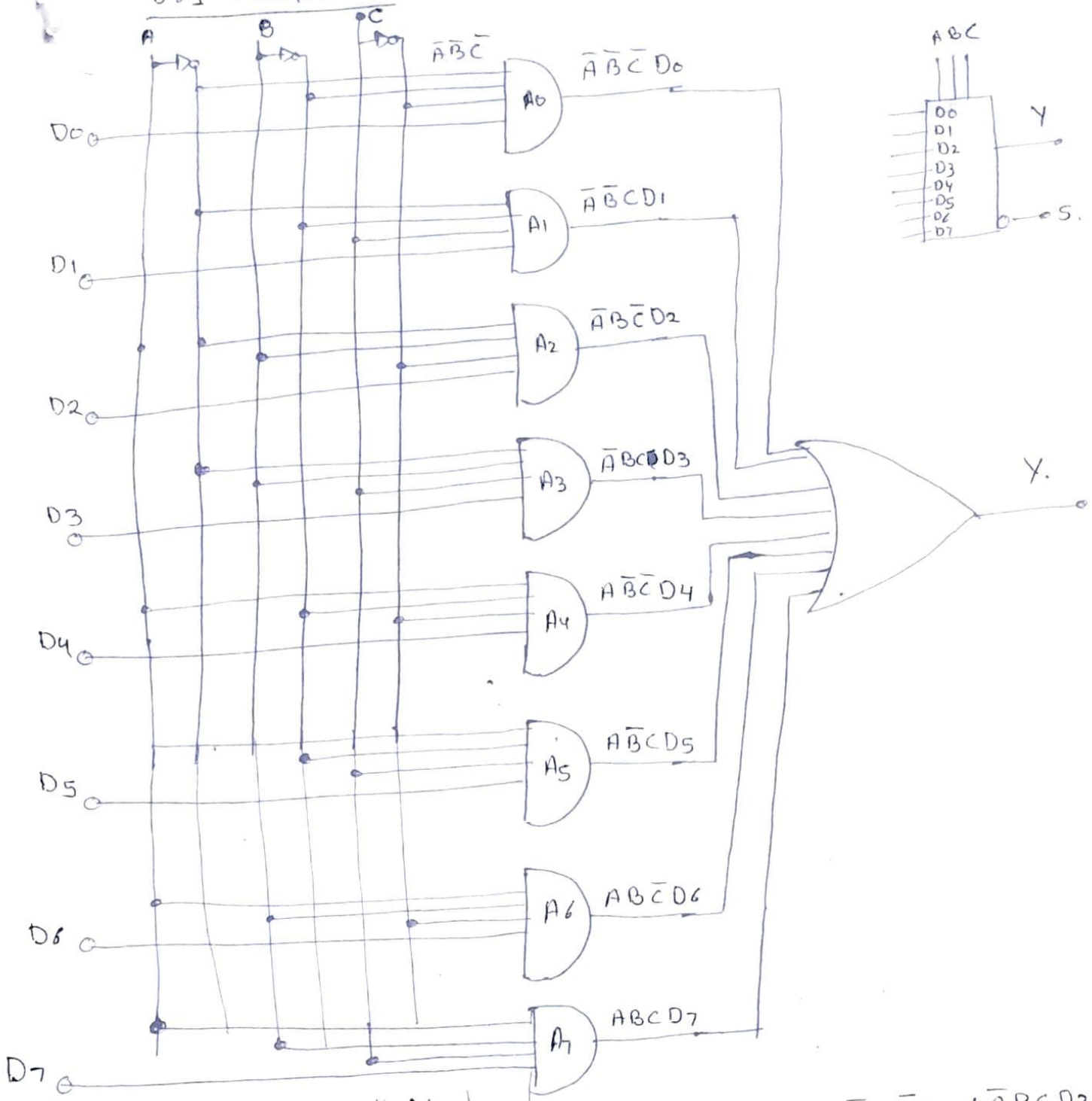
$A = 1, B = 0,$

AND gate A_2 enabled, and A_0, A_1 and A_3 disabled $Y = D_2$

$A = 1, B = 1.$

A_3 enabled and A_0, A_1, A_2 disabled $Y = D_3$.

8:1 Multiplexer



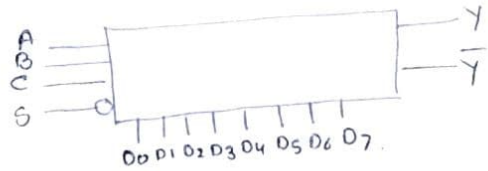
S	A	B	C	Y
1	X	X	X	0
0	0	0	0	D_0
	0	0	1	D_1
	0	1	0	D_2
	0	1	1	D_3
	1	0	0	D_4
	1	0	1	D_5
	1	1	0	D_6
	1	1	1	D_7

$$Y = \bar{A}\bar{B}\bar{C}D_0 + \bar{A}\bar{B}CD_1 + \bar{A}B\bar{C}D_2 + \bar{A}BCD_3$$
$$A\bar{B}\bar{C}D_4 + A\bar{B}CD_5 + AB\bar{C}D_6 + ABCD_7$$

Advantages: ① It minimises the IC Package.
② Logic design is simplified.
③ Simplification of Boolean expression is not required.

Example: 8:1 - 74151
16:1 - 74150
4:1 - 74153
2:1 - 74157 Quad 2:1.

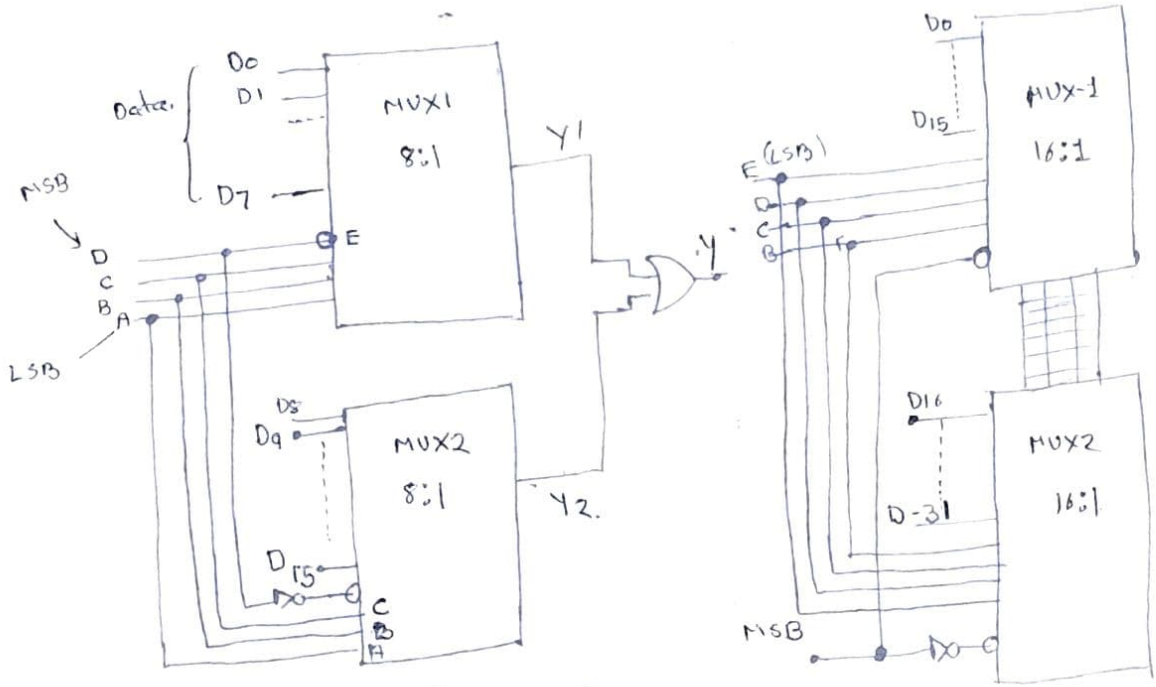
74151



Design of Higher order MUX using Lower order MUX.

16:1 using 8:1

32:1 using 16:1



MSB is connected to $\bar{E}$ of MUX1

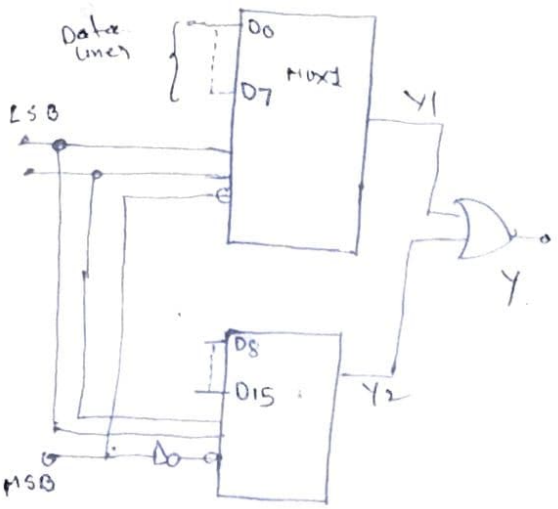
It is connected to $\bar{E}$ of MUX through inverter.

MSB = 1, MUX1 is disabled
MUX1 is enabled and D8 - D15 are multiplex to Y.

MSB = 0, MUX1 is enabled, MUX2 - Disabled.
D0 - D7 are multiplex to Y.

8:1 using 4:1

4:1 using 2:1



Applications of multiplexers:

(1) Data selection
(2) Data Routing
(3) Operation sequencing
(4) Parallel to serial conversion
(5) logic function generation.
(6) Implementation of Boolean expression: