SHIVAJI COLLEGE, UNIVERSITY OF DELHI
DEPARTMENT OF COMPUTER SCIENCE
INTERNAL ASSIGNMENT
(Academic Year 2023-24)

Name of the Course	: DSC-3	Semester	: III
Name of the Paper	: Computer System Architecture	Maximum Marks	: 20
Faculty Name	: Mr. Rakesh Yadav	Last Date of Submission: 14.12.2023	

ASSIGNMENT NO 2

Q NO1. Write your full name in ASCII using an 8 bit code with the leftmost bit always 0. Include a space between parts of name and a period at the end

Q NO2. GIVE 1's and 2's complement representation of following using 12 bit binary representation

(a) hexadecimal nos +ABC, - 2AE, +567, -A57

(b) Decimal nos - 567, - 1023, + 1011

Q NO 3. Perform the following arithmetic operations using signed 2's complement representation for negative numbers. Use 8 bit representation

(i) (+41) +(-12)

(ii) (-42)-(-13)

(iii) (+72)+(+80)

(iv) (-72) +(+80)

Q NO 4. Perform the following arithmetic operations using signed 1's complement representation for negative numbers. Use 8 bit representation

(i) (+41) +(-12)

(ii) (-42)-(-13)

(iii) (+72)+(+80)

(iv) (-72) +(+80)

Qno5. The outputs of four registers, R0,R1,R2 and R3, are connected through 4 to 1 line multiplexers to the inputs of a fifth register R5. Each register is 8 bits long. The required transfers are dictated by four timing variables T0 – T3 as follows

T0: R5 <- R0

T1: R5 <- R1

T2: R5 <- R2

T3: R5 <- R3

The timing variables are mutually exclusive, which means that only one variable is equal to 1 at any given time, while the other three are equal to 0. Draw a block

diagram showing the hardware implementation of the register transfers. Include the connections necessary from the four timing variables to the selection inputs of the multiplexers and to the load input of register R5.

QNO 6. Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry Cin. Draw the logic diagram for the first two stages

1. S=0 and Cin = 0 D = A – 1
2. S=0 and Cin = 1 D = A + 1
3. S=1 and Cin = 0 D = A + B
4. S=1 and Cin = 1 D = A - B

Here D is output.

Faculty Signature